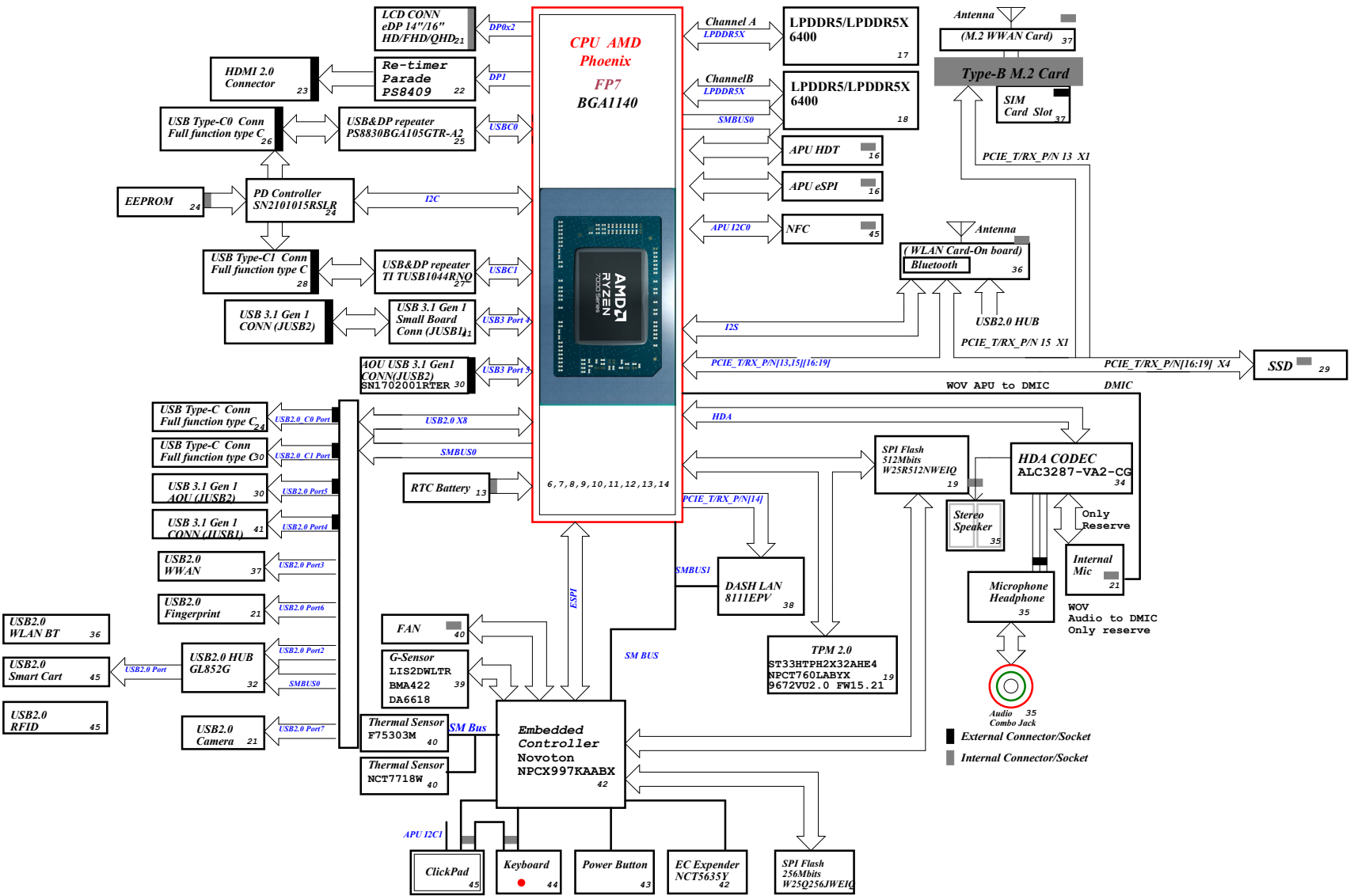
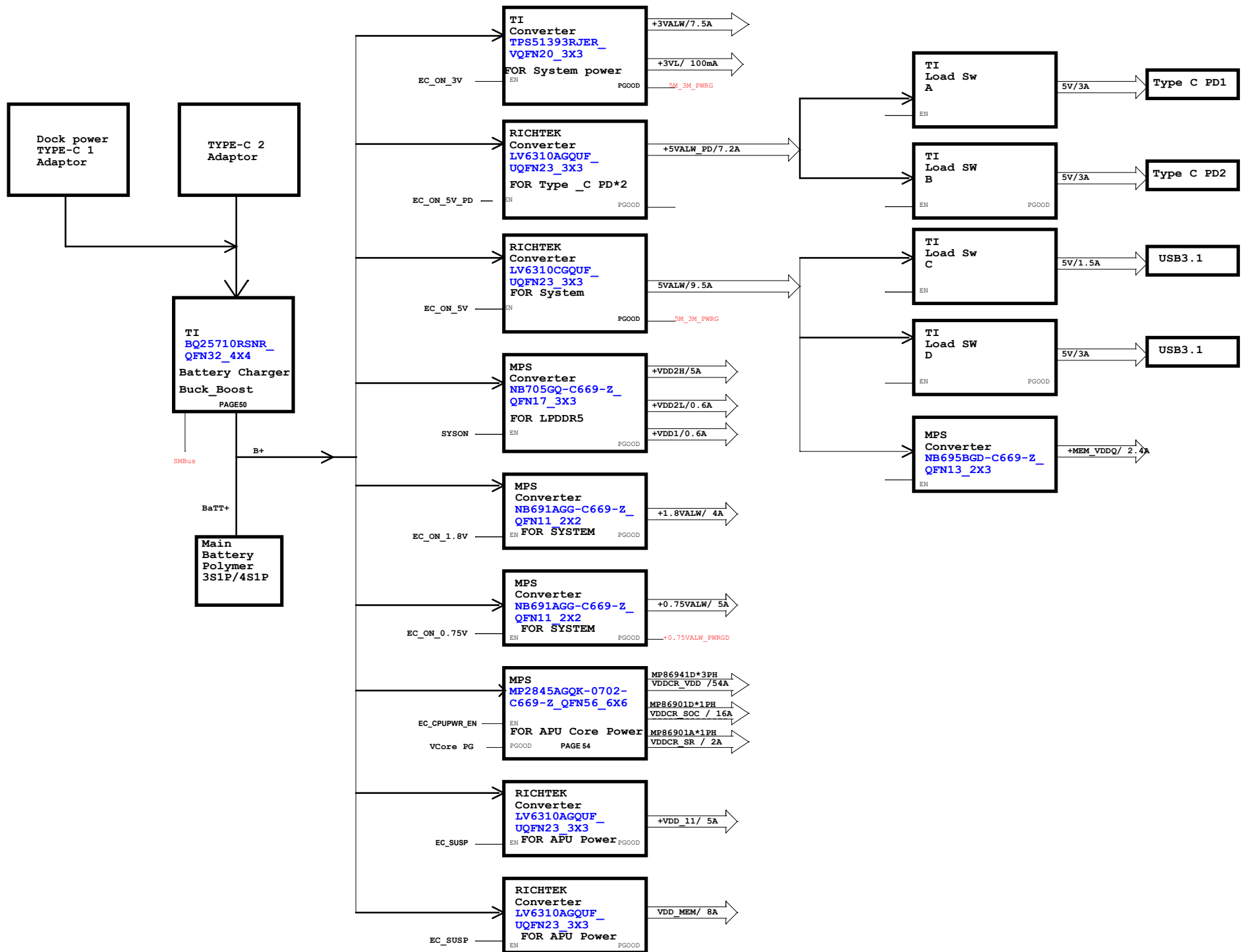


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 P060-Change List_EE
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PD I2C address table

Port	Master	Slave	End Port	Address	Description
I2C_EC	EC	PD	PORTA	0x23	ADCIN1=0.057#1 ; ADCIN2=1#7 ADCIN1 decoded value = 1 ADCIN2 decoded value = 7 I2C address index = #4 A port: 0100011 B port: 0100111
			PORTB	0x27	
I2C2S	NC	NC	PORTA	0x23	NC
			PORTB	0x27	
I2C3M	PD	APU	PORTA-TypeC1	0x54	The USB PD I2C Slave responds to a 7-bit address.
			portb-TypeC0	0x58	
	PD	TYPEC1-5460	PortA-5460	0X1F	[PIN35,38]: LL: 0X10; HH: 0X1F
		TYPEC0-8830	portB-8830	0X18	[GPI01,GPI00] : LL:0x10/0x11; LH:0x20/0x21; HL:0x30/0x31; HH:0x40/0x41;

EC I2C address table

Port	Master	Slave	End Port	Address	Description
SDA1A SCL1A	EC	P sensor	P sensor	0x44	The I2C device has a 7 bit Slave Address (default 0x44H) in the control byte
SDA2A SCL2A	EC	Expander1	Expander1		The I2C Slave address is {0100,A2,A1,A0,R/W} Address:0100101R/W
	EC	Expander2	Expander2		Address:0100110R/W
	EC	Expander3	Expander3		Address:0100010R/W
SDA2B SCL2B	EC	HDMI	HDMI	0x10 - 0x2F	
	EC	Audio	SN6147	0x66	
	EC	APU	APU Thermal	0x98	confirm with David Liu
SDA3A SCL3A	EC	VRM	VRM	0x20	To support multiple VR devices used with the same PMBusTM interface, PMBusTM address programming either by ADDR
	EC	CHARGER	CHARGER	0x12	The device performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus.
	EC	Battery	Battery		Need Battery support
SDA4A SCL4A	EC	TS 1	TS 1	0x4D	1001_101xb
	EC	TS 2	TS 2 (SMBUS)	0x4C	NCT7718W I2C/ SMBusTM address is 1001100xb
	EC	G sensor	G sensor (I2C)		The Slave Address (SAD) associated to the LIS2DWL is 001100xb where the x bit is modified by the SA0/SDO pin in order to modify the device address(0011000)
SDA5A SCL5A	EC	PD	PD	N/A	The I2C slave address is {0,1,0,0,1,1,0,W/R} (Miramema)
SDA6A SCL6A	EC	TYPEA Port Debug	TYPEA		Refer to PD table
	EC	TYPEC Port Debug	TYPEC		

APU I2C address table

Port	Master	Slave	End Port	Address	Description
I2C0	APU				
		T_PANEL	T_PANEL	0x10 ELAN 0x09 Siliconworks 0x40/0x10 G2	
I2C1	APU	NFC	NFC	0x29	
	APU	CP	CP	0x15	
I2C2	APU	8830 I2C	8830 I2C	0x20	
	APU	USB Hub	USB Hub	0x2C	
I2C3 (SMBUS)	APU	DASH LAN	DASH LAN		
SFB_I2C	APU	NC	NC	NC	
	APU	NC	NC	NC	

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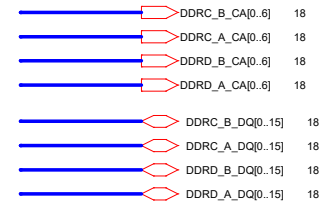
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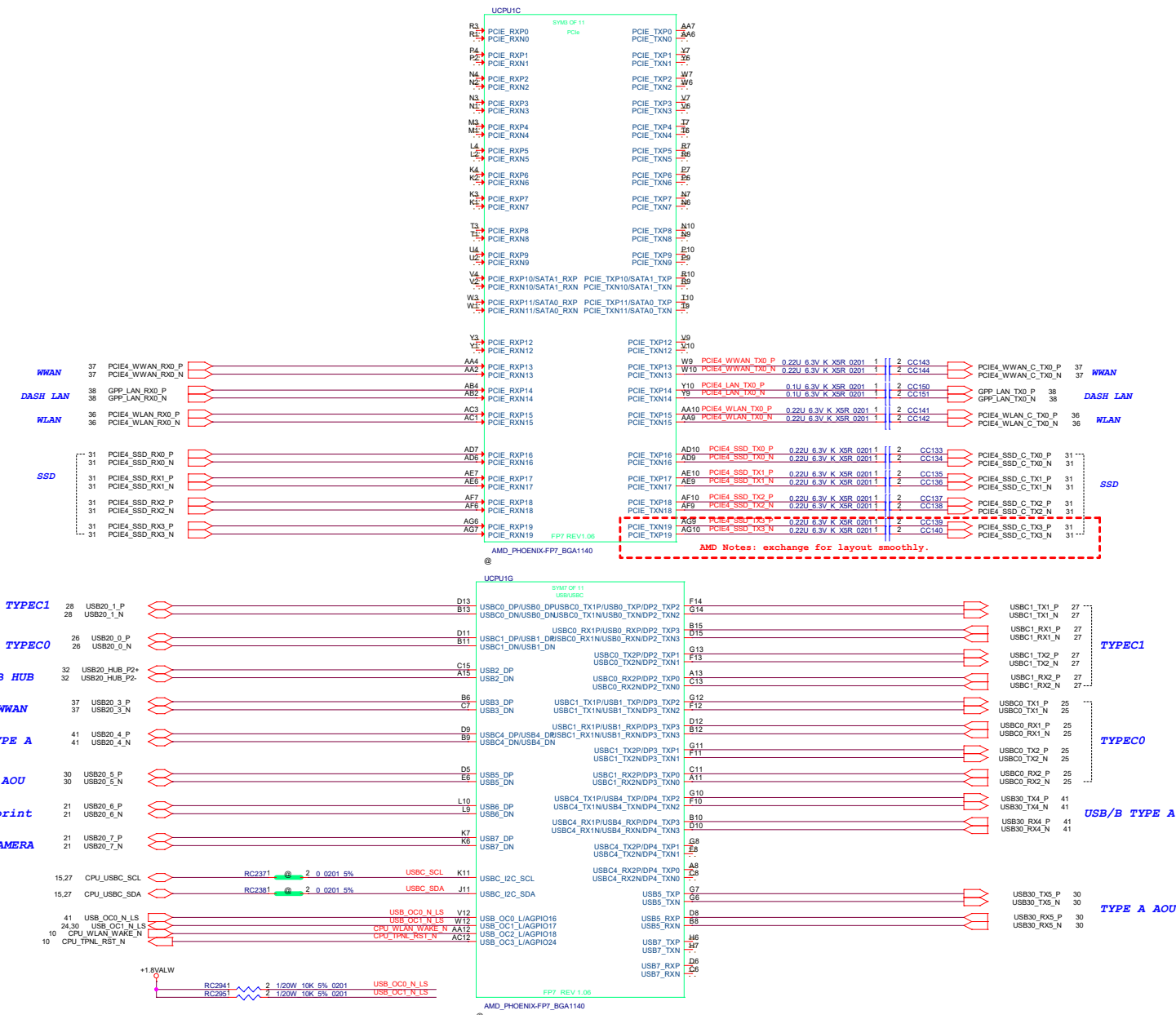
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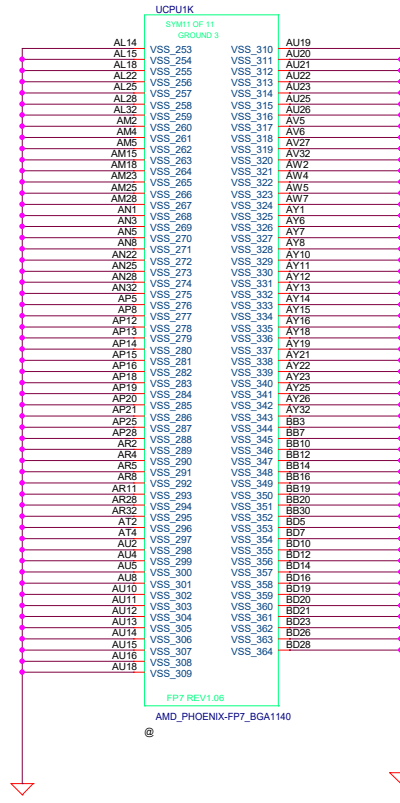
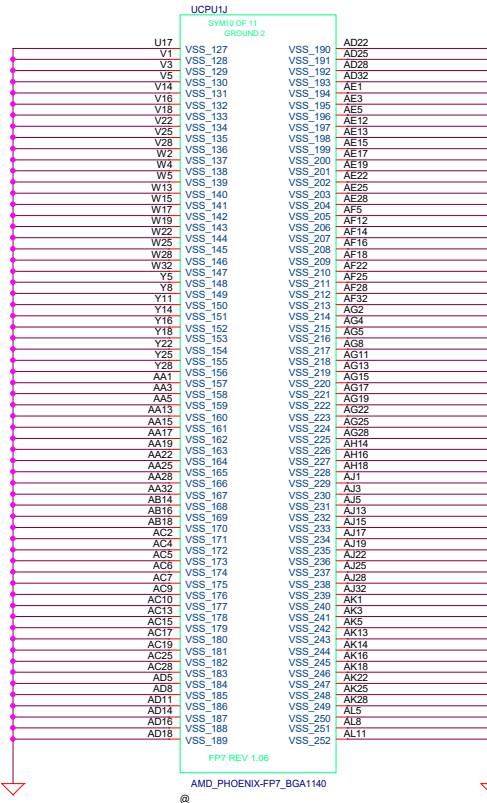
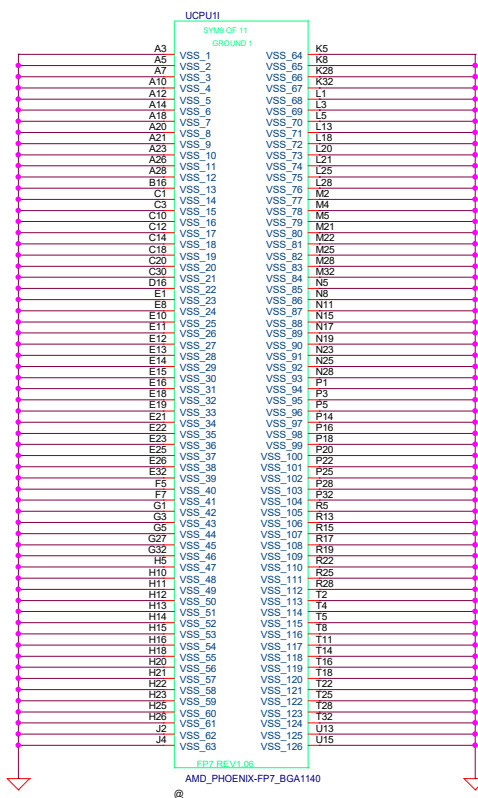
Map/SMBUS/HSIO

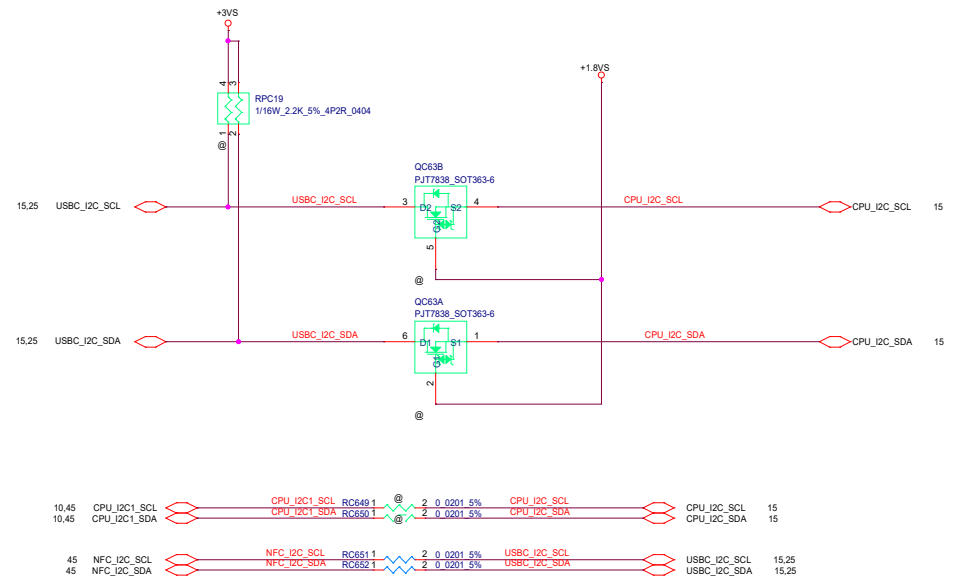
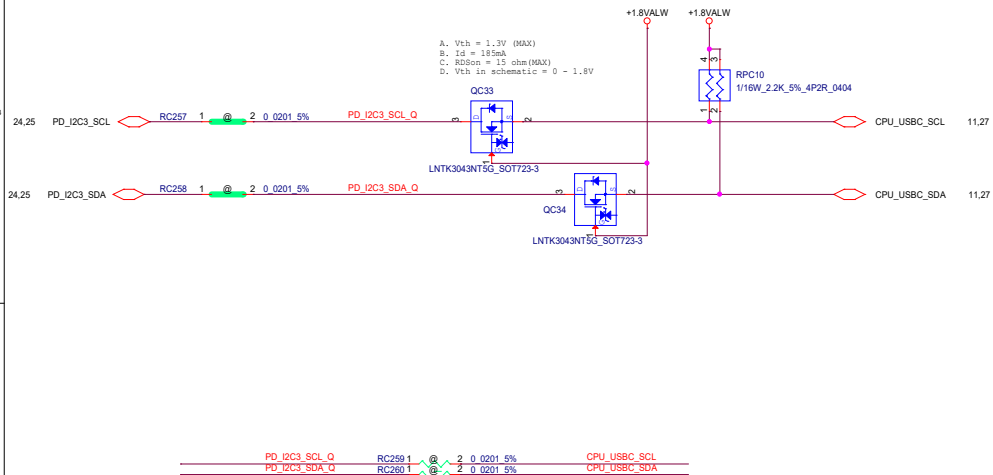
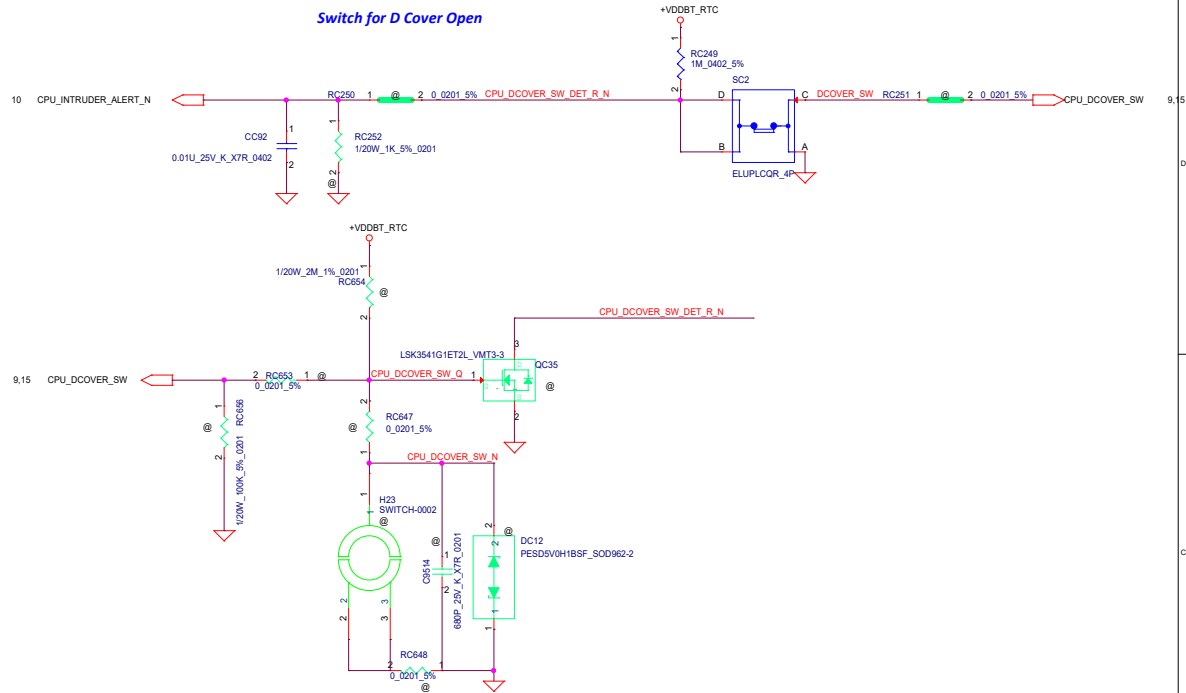
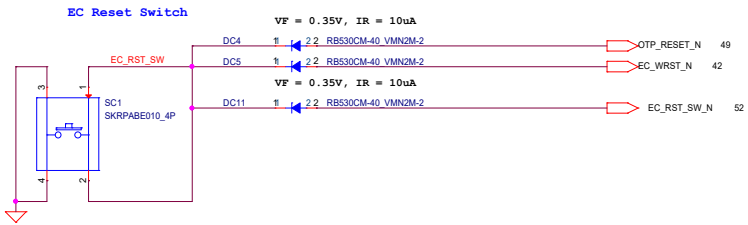
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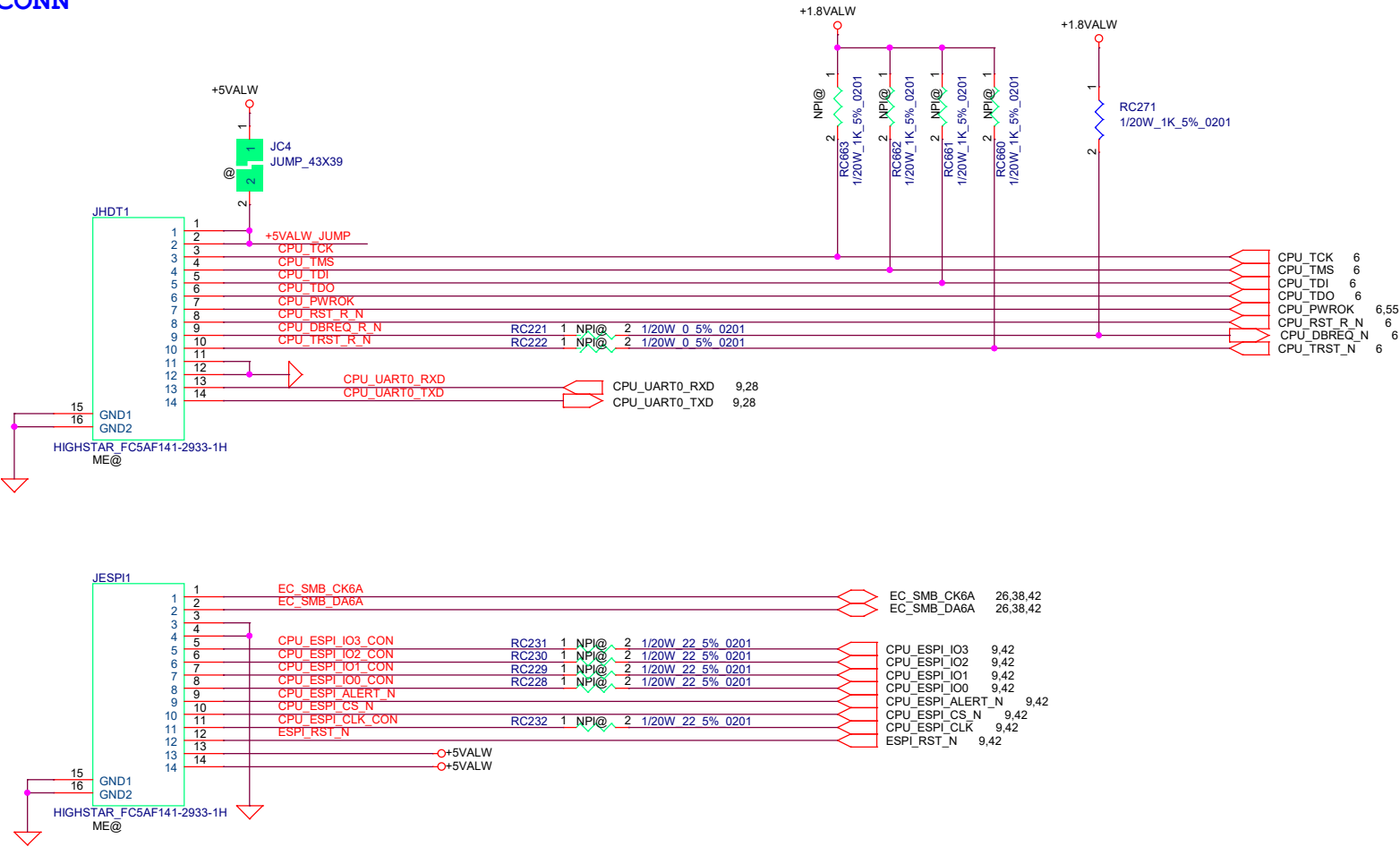
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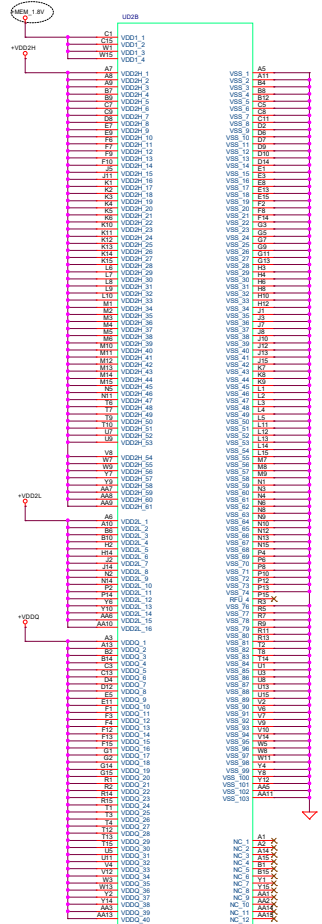
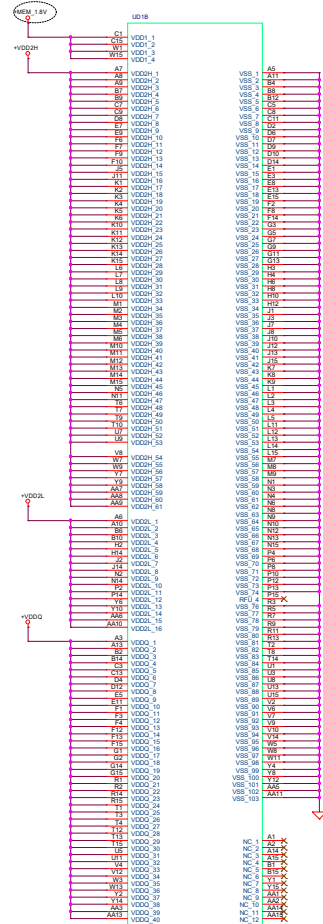
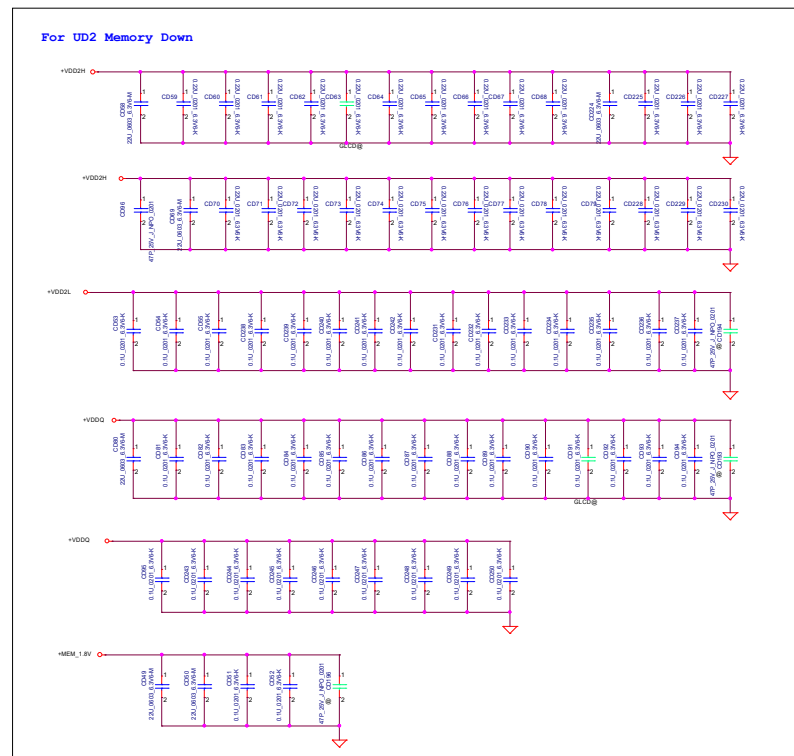
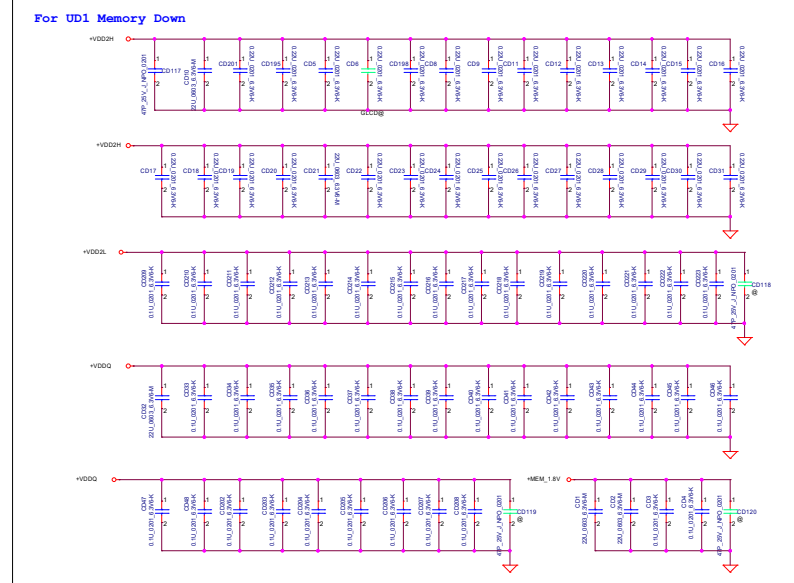
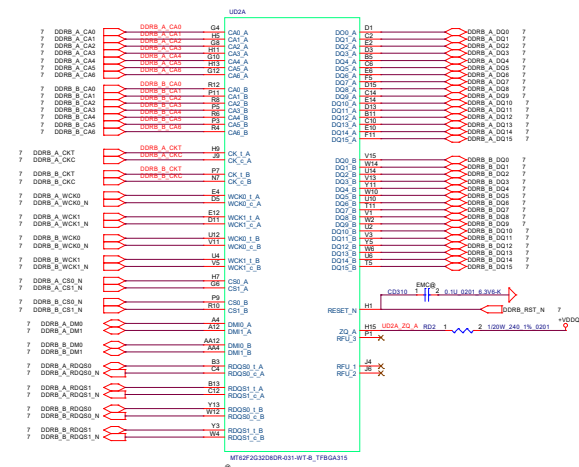
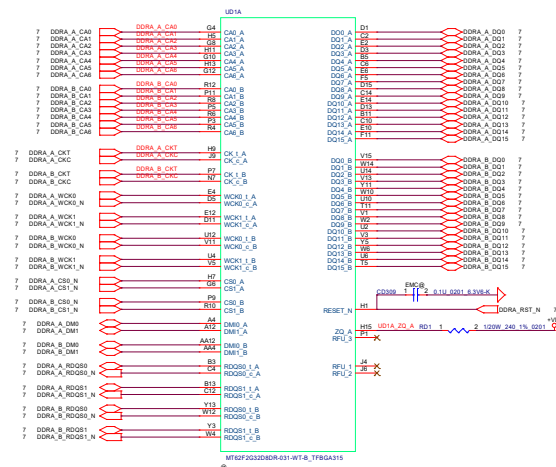


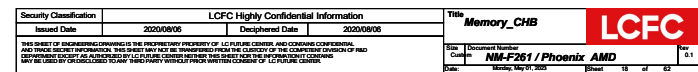
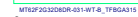
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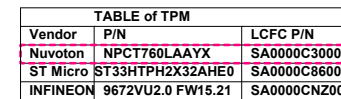


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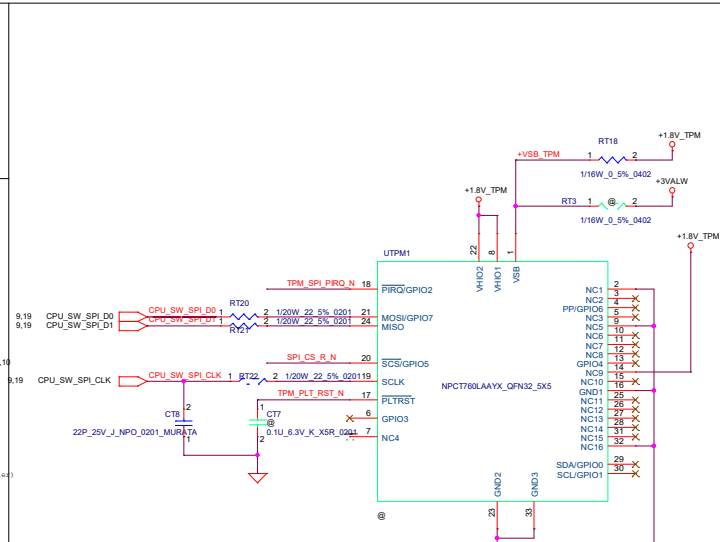




Timing diagram showing the relationship between VDD, VSB, and SPI_RST# signals. The diagram includes a note regarding the timing requirements for SPI_RST# and VSB power-up.

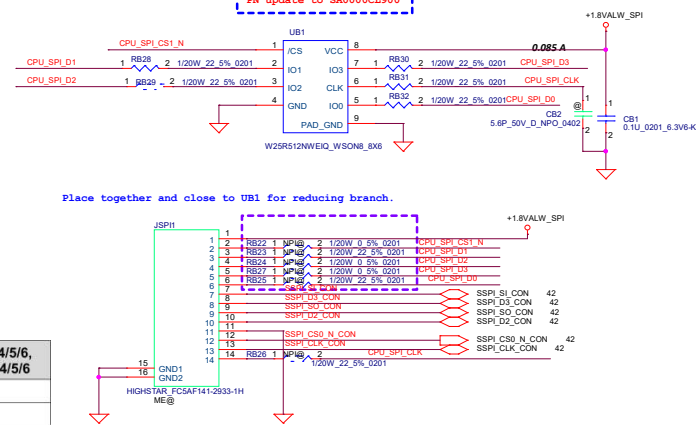
NOTE:

- 1) SPI_RST# is recommended to connect the VSB to the system's standby voltage to improve performance.
- 2) SPI_RST# must be asserted for at least 5 msec after VSB power-up.
- 3) VSB may come up anytime before VDD power-up, but not after VDD power-up.
- 4) SPI_RST# may be asserted together with VDD power negation, but should not be at any point exceed 0.5V above the VDD power level.

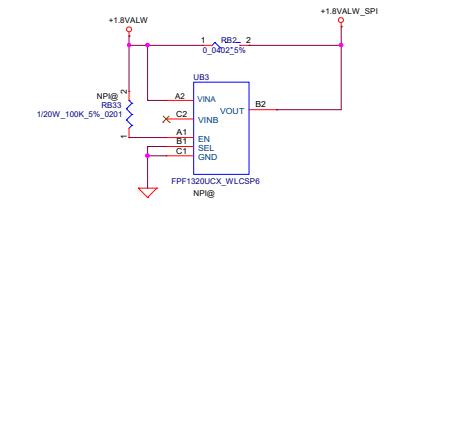



Pin No	Nuvoton NPC7T60LAAYX	ST Micro ST33HTFH2X32AHE0	INFINEON SLB9670VQ2.0F.W7.85
1	VSB	NIC	NCI/VDD
2	NC	GND	GND
3	NC	NIC	NCI
4	GPIO/PP	NIC	NCI
5	NC	NIC	NCI
6	GPIO3	GPIO_LP	GPIO
7	NC	GPIO_PP	PP
8	VHIO	NIC	VDD
9			
10	NC	NIC	GND
11	NC	NIC	NCI
12	NC	NIC	NCI
13	NC	NIC	NCI
14	GPIO4	NIC	NCI
15	GPIO	NIC	NCI/VDD
16	NC	NIC	NCI
	GND	NIC	NCI/VDD
17			
18	RLTRST#	SPL_RST#	RST#
19	PIRQ#/GPIO2	SPI_PIRQ#	PIRQ#
20	SCLK	SPI_CLK	SCLK
21	SCS#/GPIO5	SPI_CS#	CSS#
22	MOSI/GPIO7	MOSI	MOSI
23	VHIO	VPS	VDD
24	GND	NIC	GND
	MISO	MISO	MISO
25			
26	NC	NIC	NCI
27	NC	NIC	NCI
28	NC	NIC	NCI
29	NC	NIC	NCI
30	SDA/GPIO0	NIC	NC
31	SCL/GPIO1	NIC	NCI
32	NC	NIC	NCI
	NC	NIC	GND

PN update to SA0000CL900



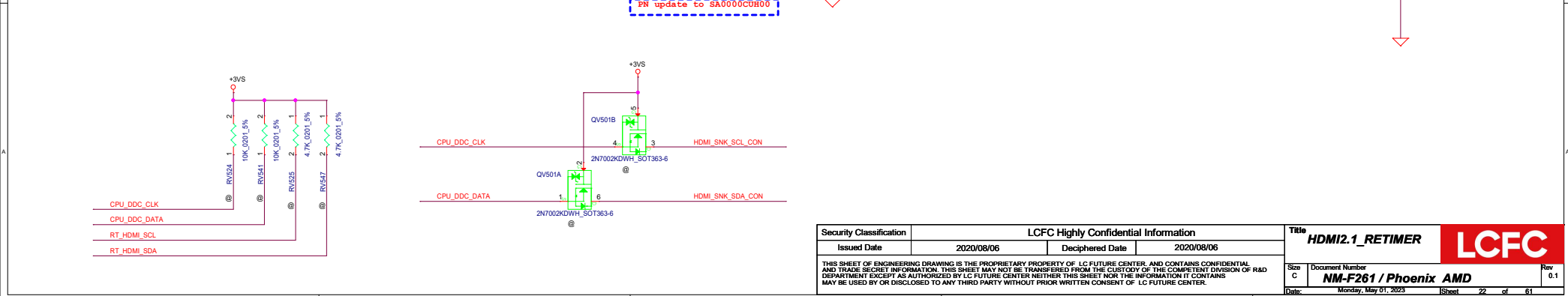
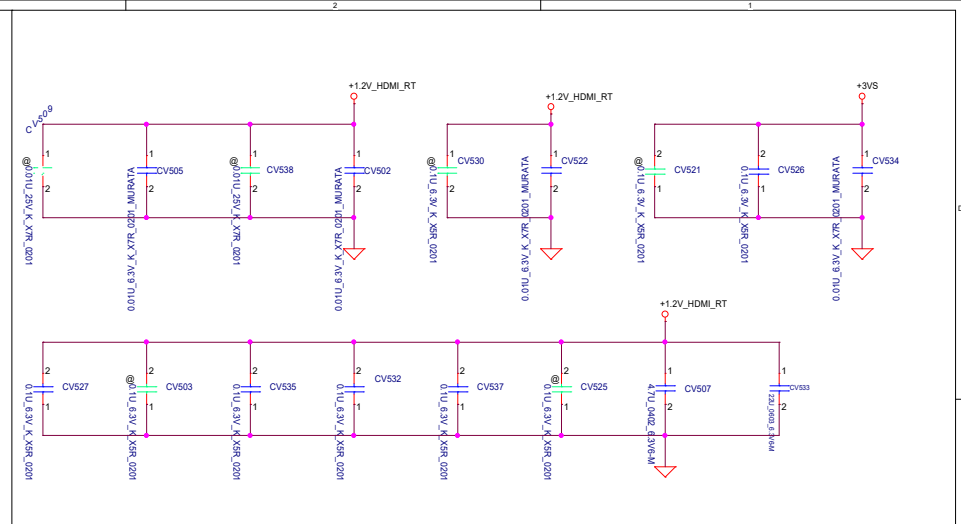
EN	IN1	IN2	NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

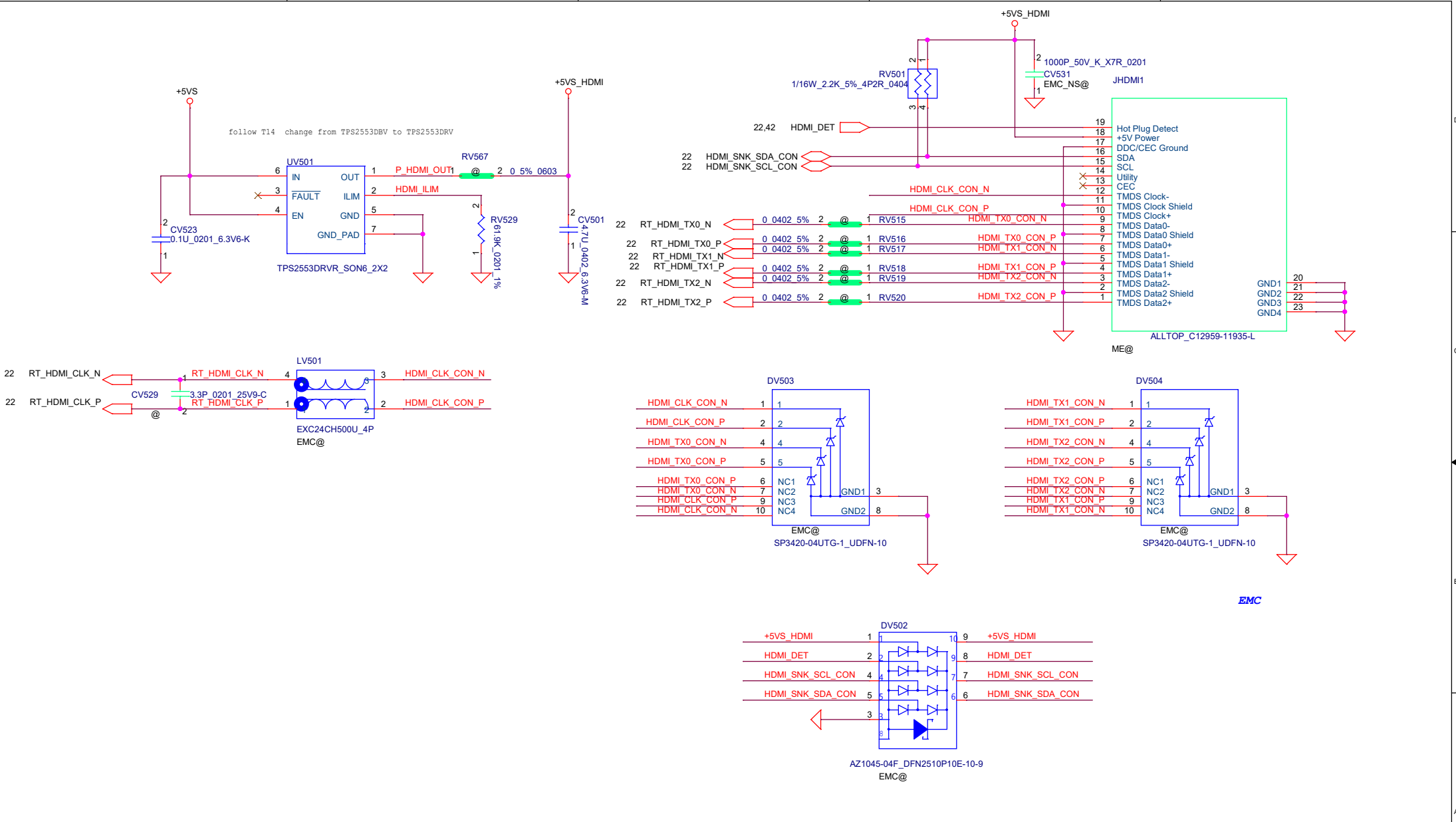


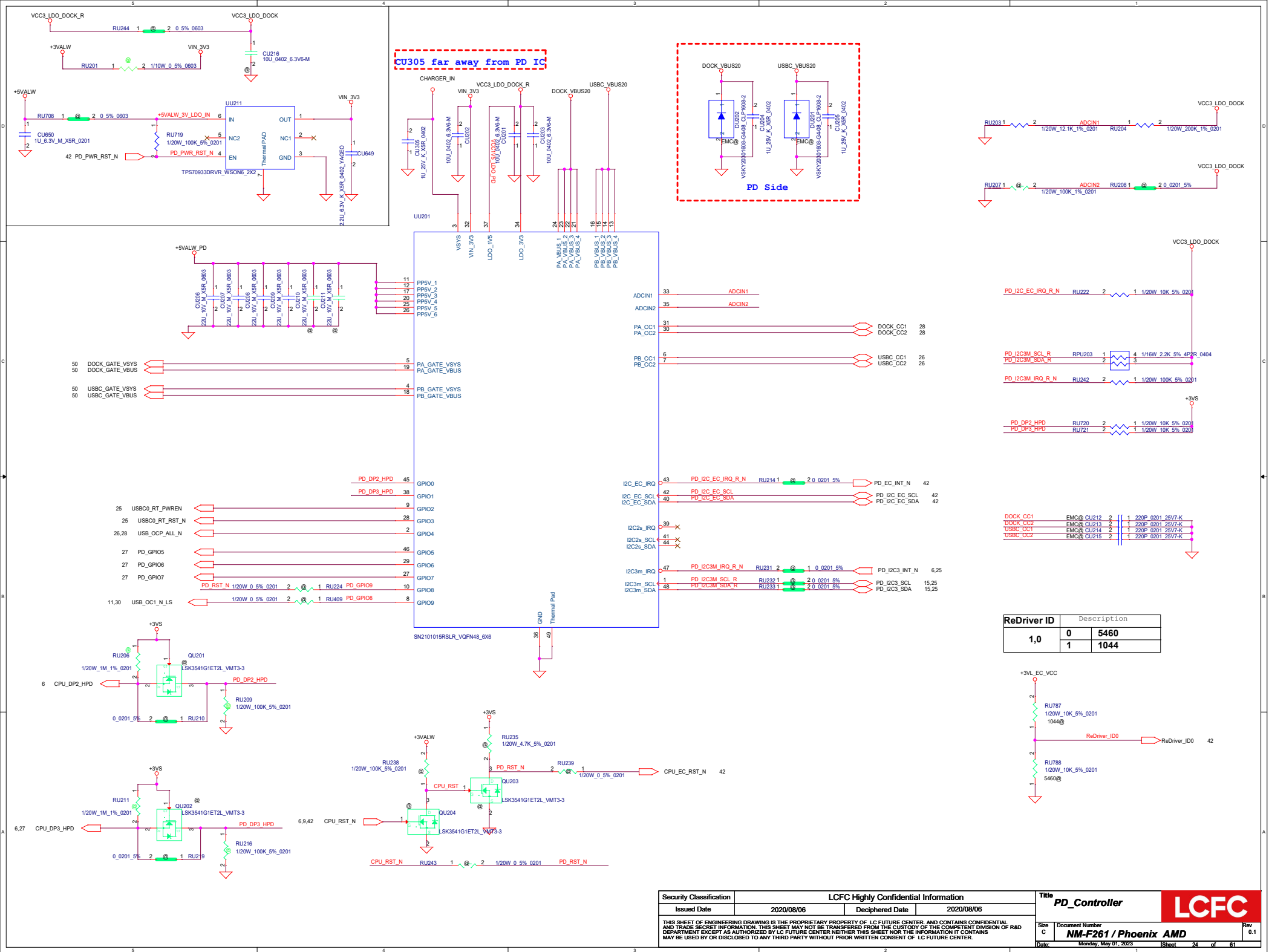
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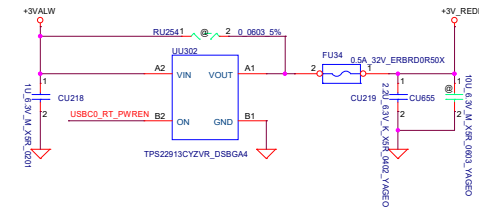
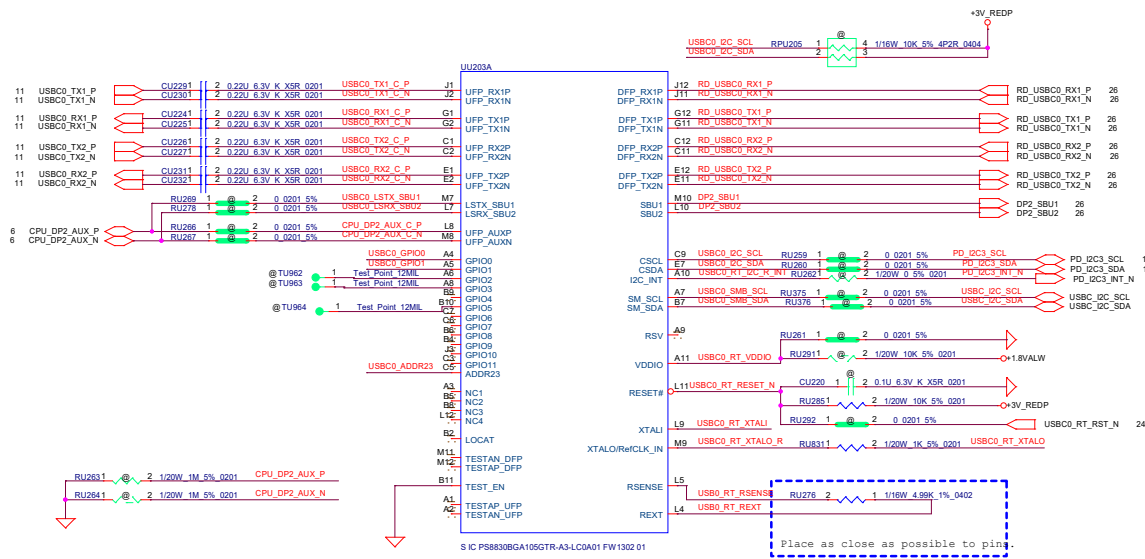
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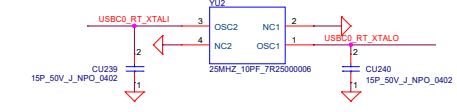






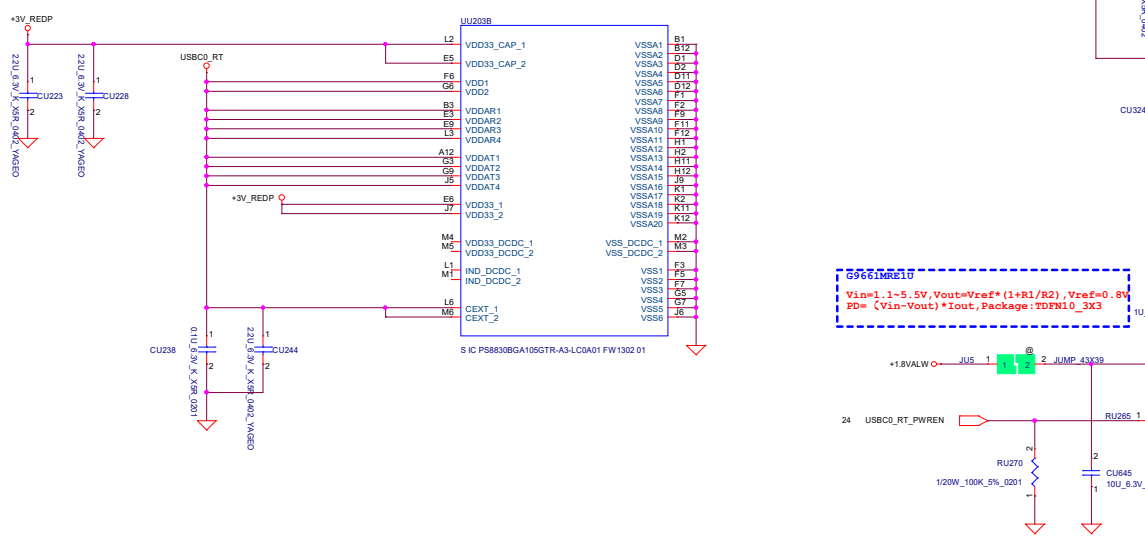


TPS22913CZVR
 Active H
 Input/output voltage range:1.4V-5.5V
 Ron=74mohm
 Rating current/OCF threshold=2.5A
 Ton=2344us
 Reverse current threshold=0.044V/Ron=0.595A



I2C: 0X30

For PS9830:I2C slave Address
 [ADDR1,ADDR0]=[GPIO1,GPIO0]
 LL:0x10/0x11; LH:0x20/0x21; HL:0x30/0x31; HH:0x40/0x41;



5551MRE17
 Vin=1.1-5.5V, Vout=Vref*(1+R1/R2), Vref=0.6V
 PD= (Vin-Vout)*Iout, Package: TDFN10_3X3

Vout (V)	R1 (KΩ)	R2 (KΩ)
1.15	12.7	28.7

1.15V 1.8A For PS8830

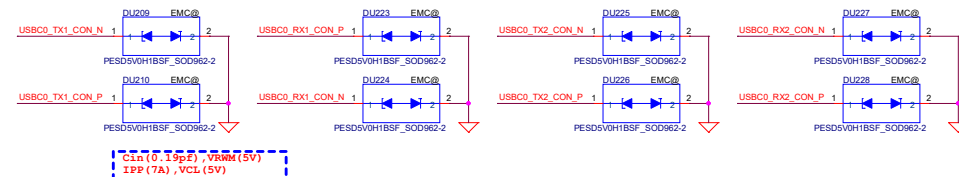
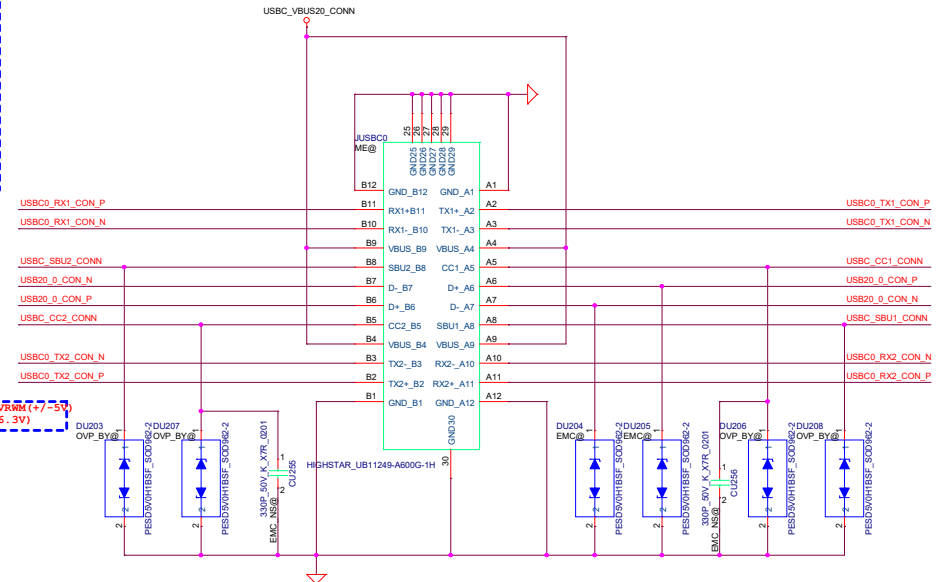
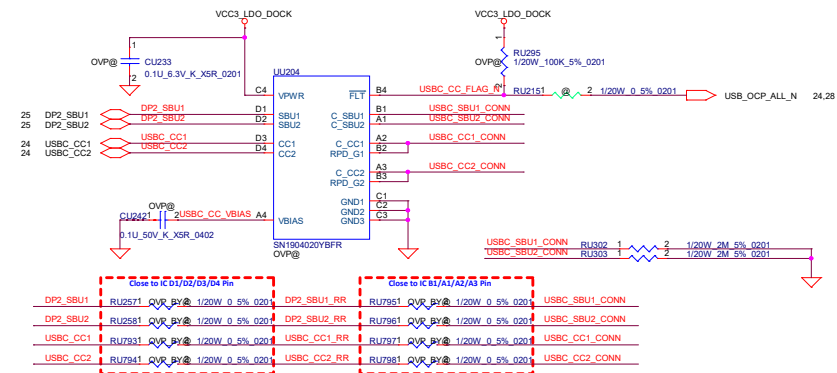
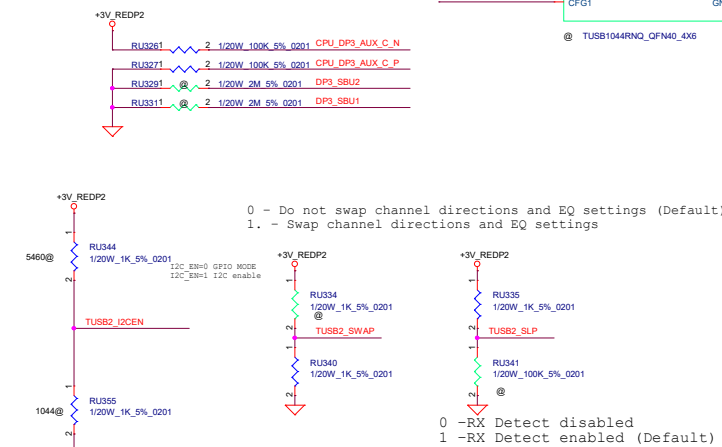




TABLE of DIR/EQ		
	1044	5460
RU763	1K	1K/200K/47K
RU766	1K	1K
RU761	@	1K/200K/47K
RU765	1k	1K
RU762	@	1K/200K/47K
RU764	1k	1K



- 0 - Do not swap channel directions and EQ settings (Default)
- 1. - Swap channel directions and EQ settings

```
0 -RX Detect disabled
1 -RX Detect enabled (Default)
```

```
0 option1: Tie 1K 5% to GND option2:Tie directly to GND
R Tie to 20K 5% to GND
F Float(leave PIN open)
1 option1: Tie 1K 5% to VCC option2 :Tie directly to VCC
```

This PIN selects I/O voltage levels for the 2-level GPIO and I2C

0	= 3.3-V configuration I/O voltage, 3.3-V I2C interface (Default)
R	= 3.3-V configuration I/O voltage, 1.8-V I2C interface
F	= 1.8V configuration I/O voltage, 3.3-V I2C interface
1	= 1.8-V configuration I/O voltage, 1.8-V I2C interface

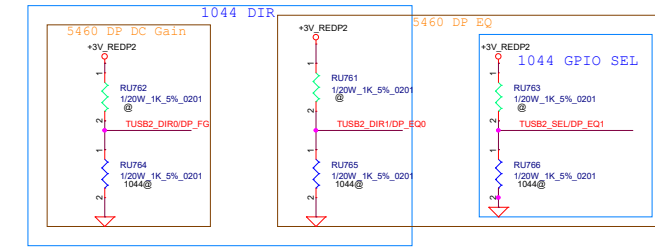
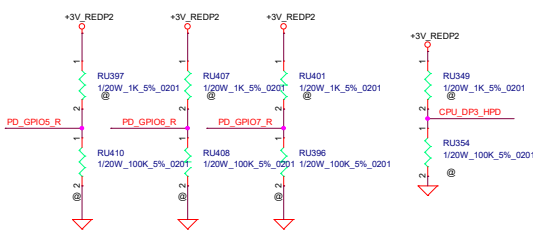


TABLE of 1044&5406		
	1044	5460
RU768	1k	1K/200K/47K
RU777	1K/20k	1K
RU769	1k	@
RU778	1K/20k	1K

TABLE of 1044&5406		
	1044	5460
RU771	1k	1K/200K/47K
RU774	1K/20k	1K
RU770	1k	@
RU773	1K/20k	1K

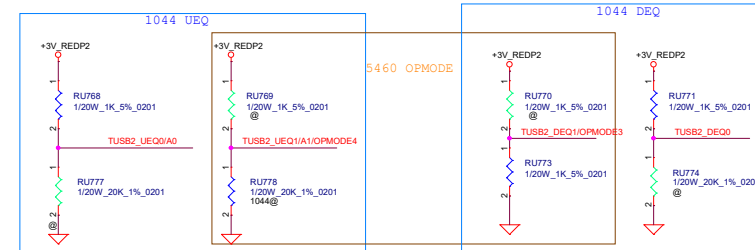
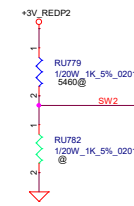
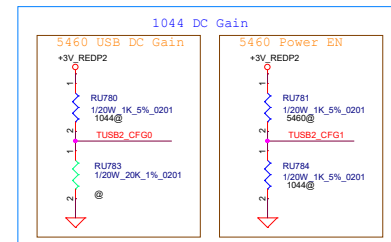
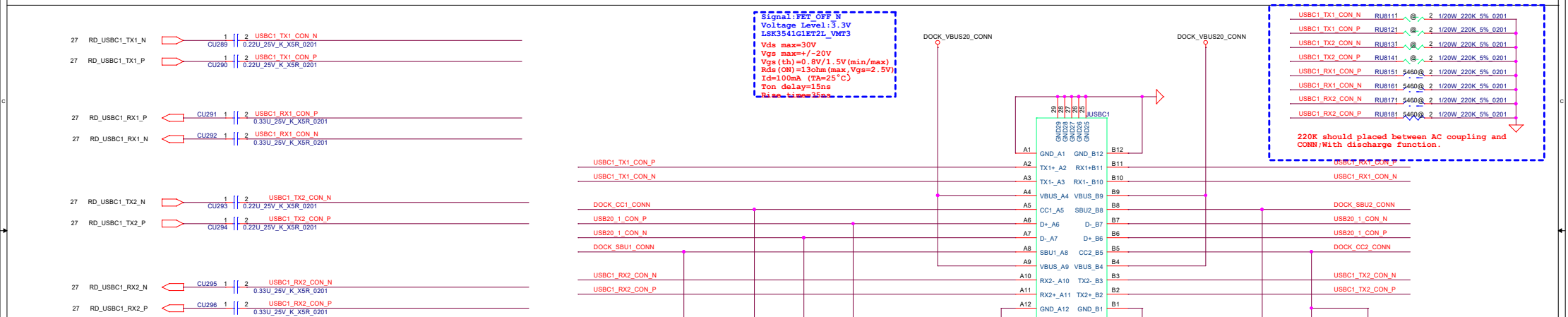
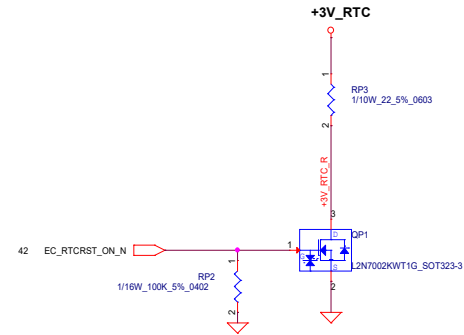
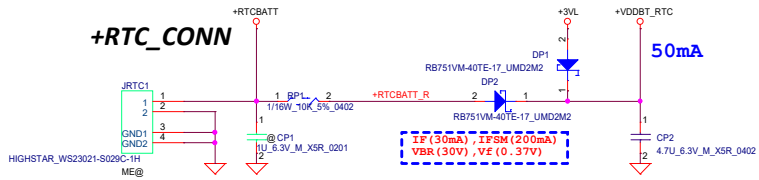
EQ setting

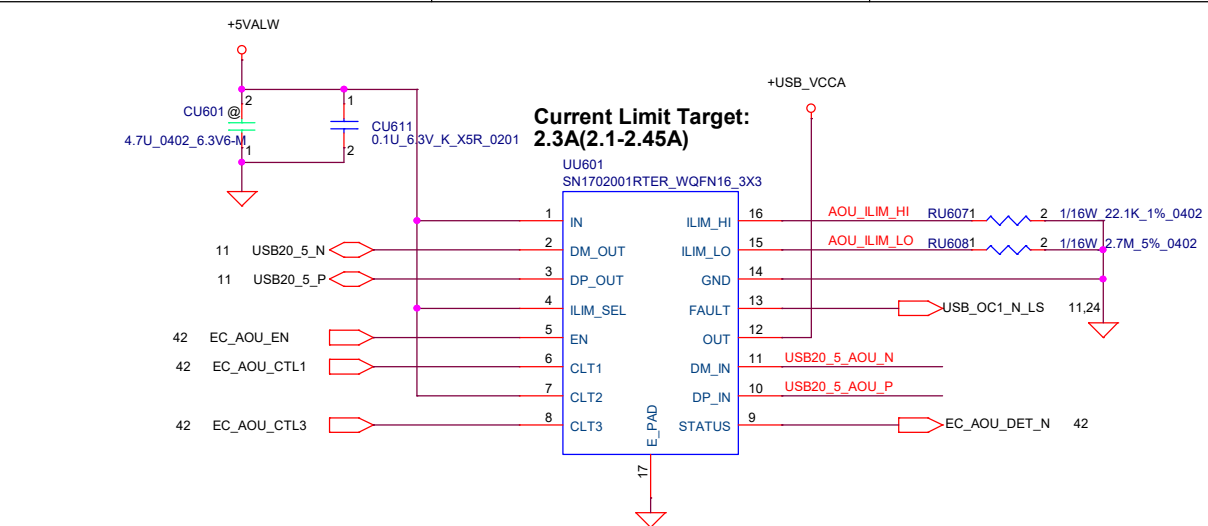
TABLE of 1044&5406		
	1044	5460
RU780	1k	1K/200K/47K
RU783	1K/20k	1K
RU781	1k	@
RU784	1K/20k	1K



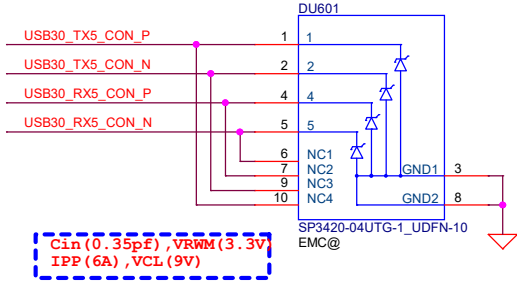
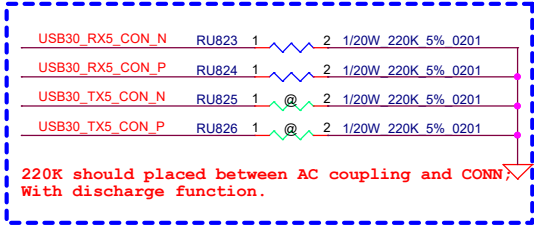




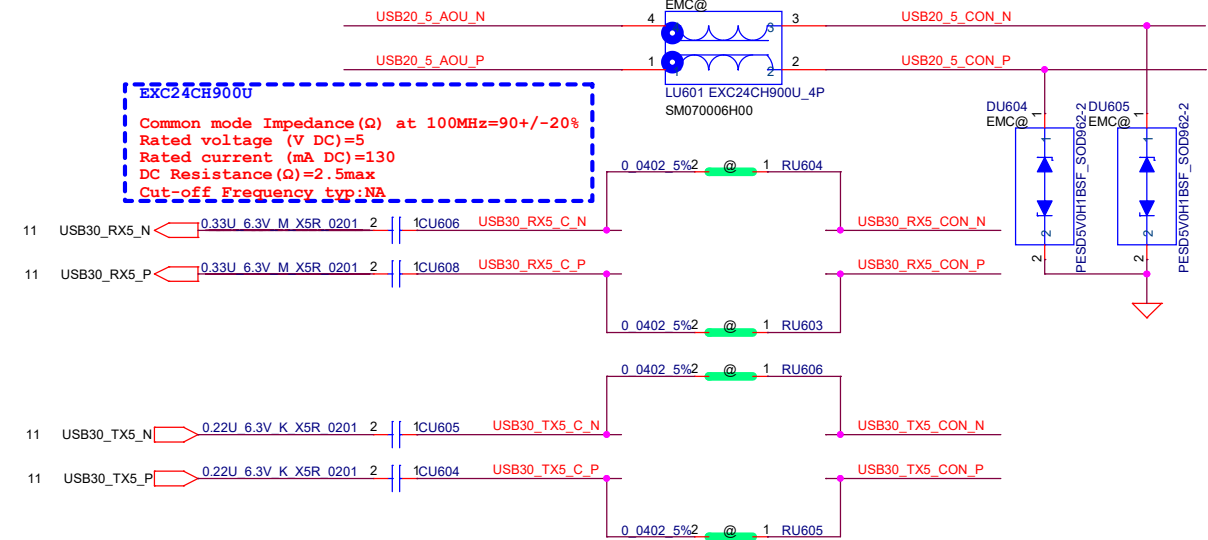
Signal: EC_RTCRST_ON_N
Voltage Level: 3.5V
L2N7002KWT1G_SOT323-3
Vds max=60V
Vgs max=+/-20V
Vgs(th)=1.2V/2V(min/max)
Rds(on)=2.7ohm(max, Vgs=5V)
Id=380mA (TA=25°C, t<Gse)
Ton delay=3.8ns
Rise time=3.4ns



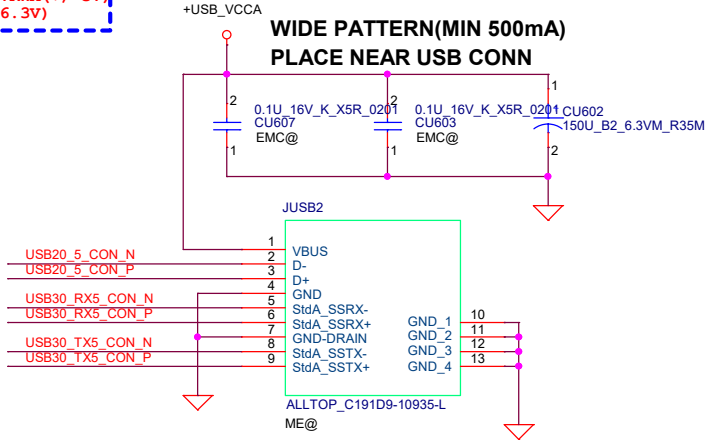
Current Limit Target:
2.3A(2.1-2.45A)

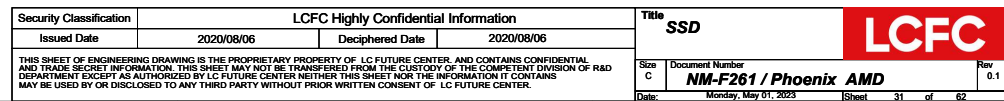
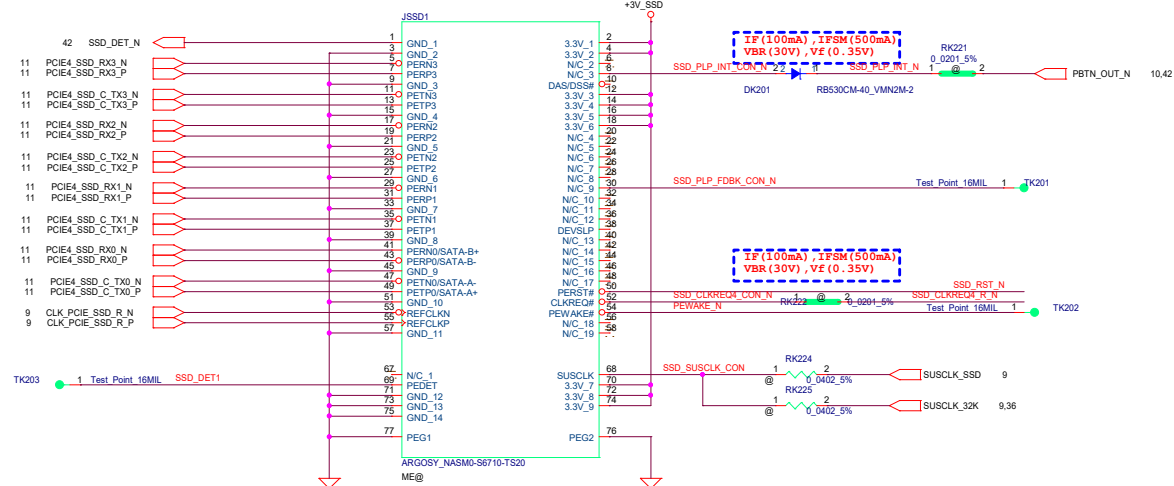
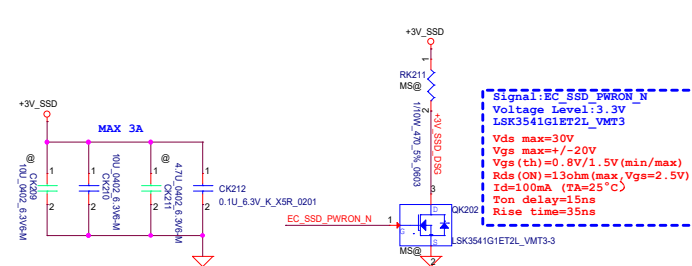


EXC24CH900U
Common mode Impedance(Ω) at 100MHz=90+/-20%
Rated voltage (V DC)=5
Rated current (mA DC)=130
DC Resistance(Ω)=2.5max
Cut-off Frequency typ:NA

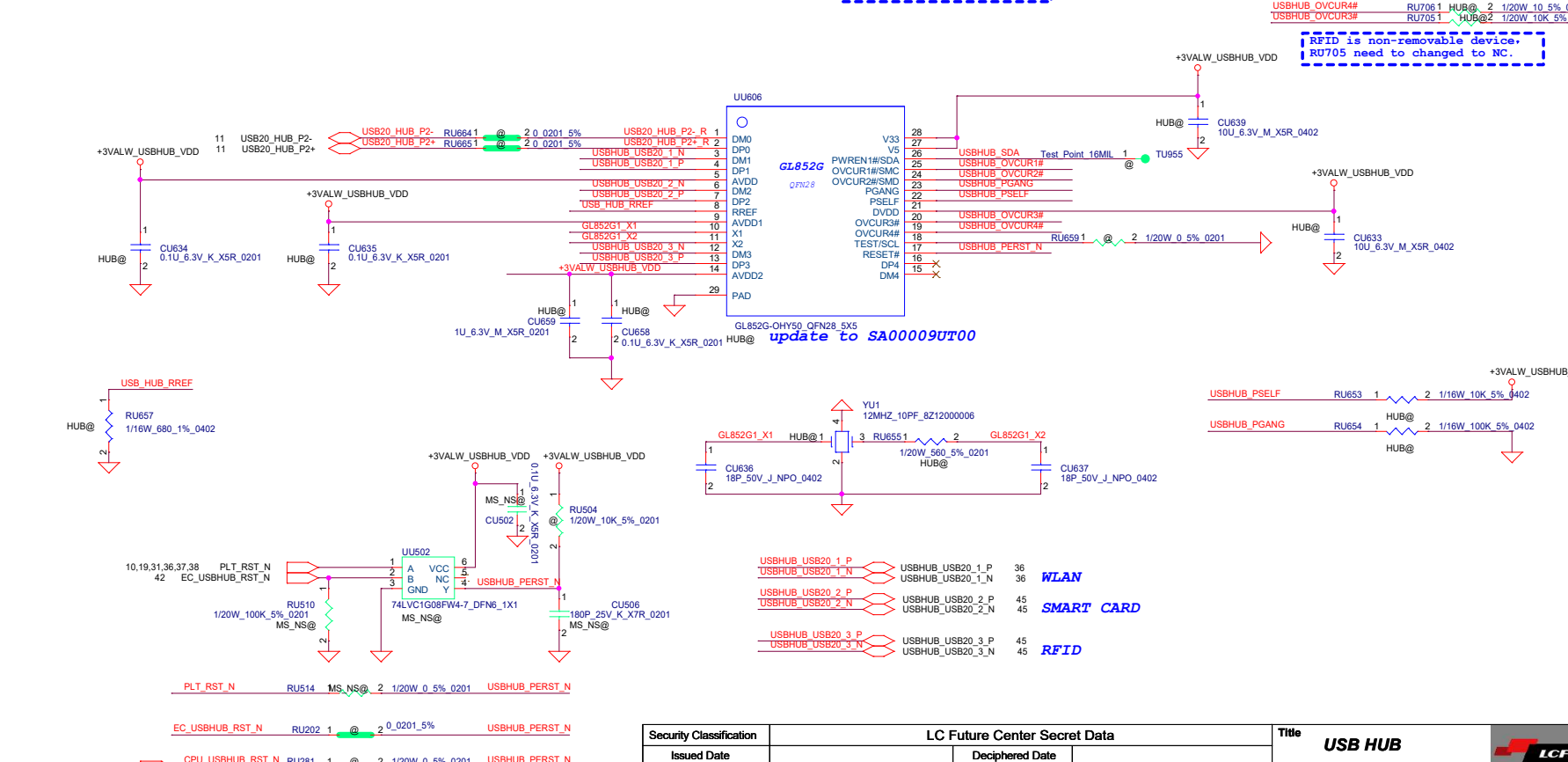
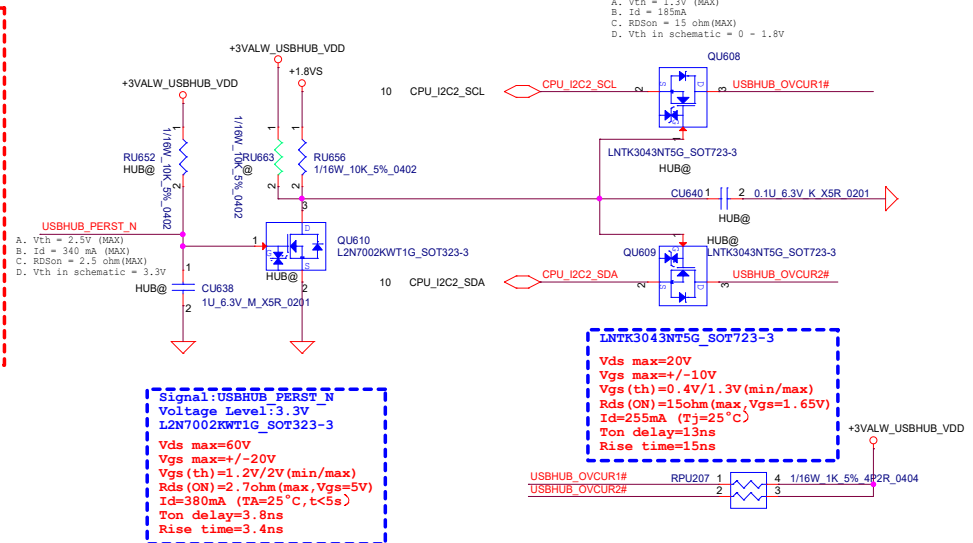
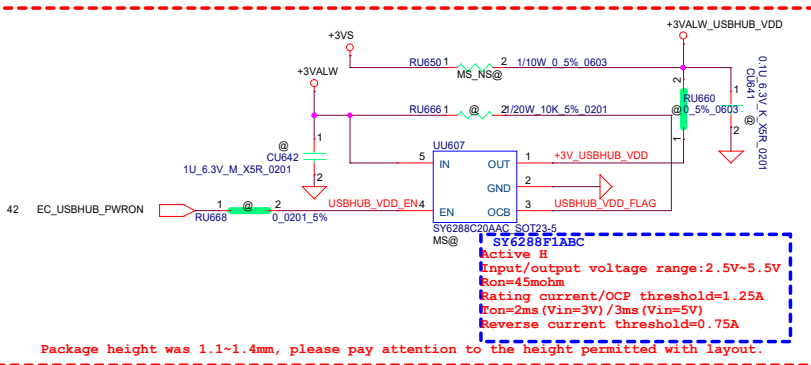


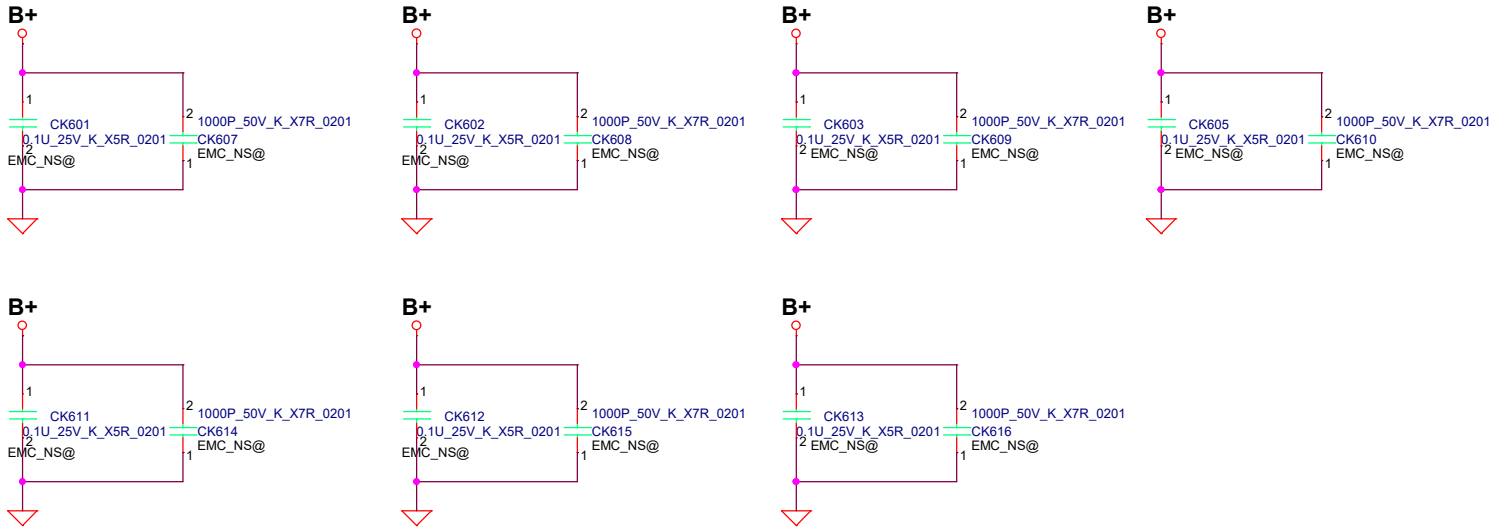
Cin(0.19pF),VRWM(+/-5V)
IPP(7A),VCL(6.3V)





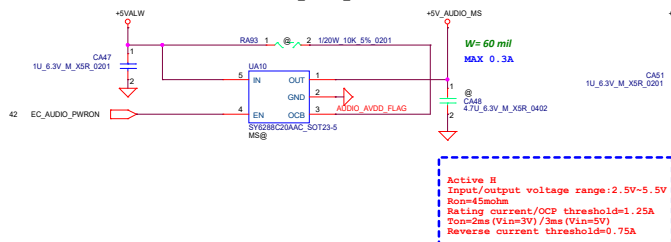
+3VALW TO +3VALW_USBHUB_VDD



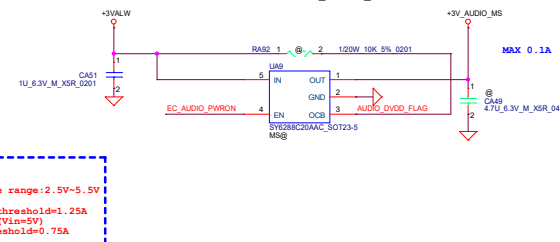


Security Classification		LCFC Highly Confidential Information				Title		<div>LCFC</div>			
Issued Date		2020/08/06		Deciphered Date		2020/08/06					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.						Title		EMI CAP			
						Size		Document Number		Rev	
						B		NM-F261 / Phoenix AMD		0.1	
						Date:		Monday, May 01, 2023		Sheet 33 of 61	

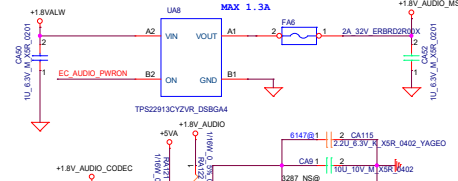
+5VALW TO +5V_AUDIO_MS



+3VALW TO +3V_AUDIO_MS



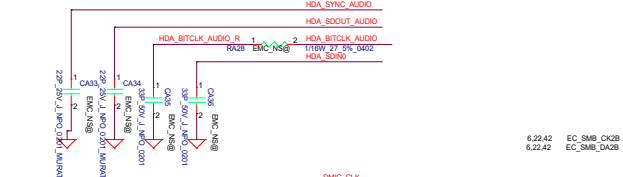
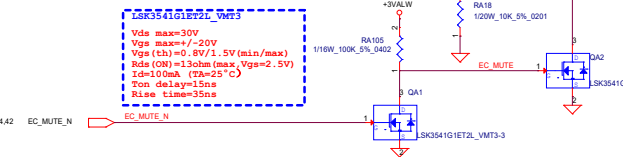
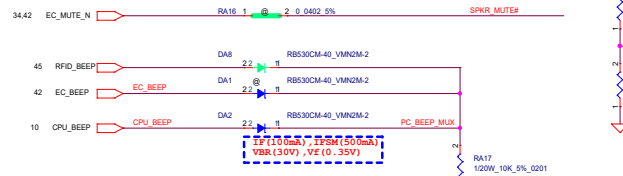
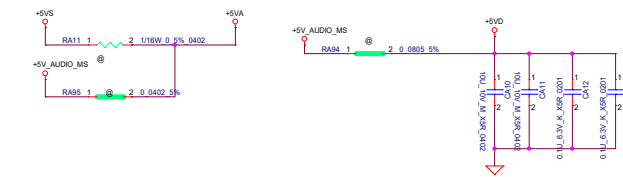
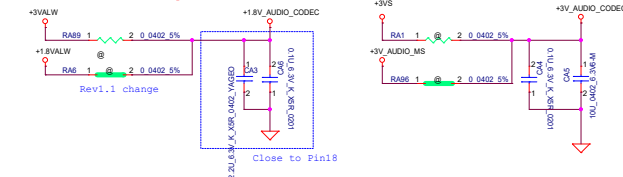
+1.8VALW TO +1.8V_AUDIO_MS



Active H
Input/output voltage range=1.4V-5.5V
Rms=740uA
Rating current/OC threshold=2.5A
Ton=2344us
Reverse current threshold=0.044V/Rom=0.595A

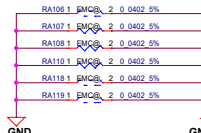
Package height was 1.1-1.4mm, please pay attention to the height permitted with layout.

Note: DVDD-I/O must be equal to or smaller than DVDD

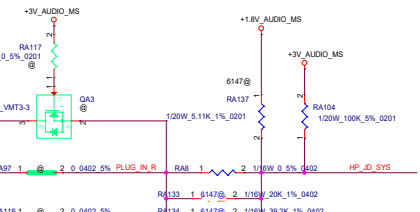


Audio Codec	Description
0	SN6147
1	ALC3287

PLACE UNDER ALC3287



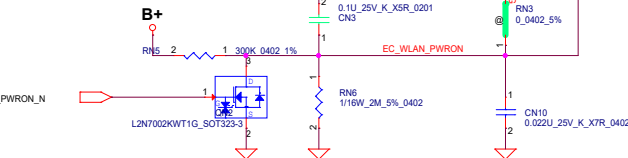
Signal: +5V_AUDIO_MS
Voltage Level: 3.3V
I_{DC} 554.101872V_VREF3
V_{DS} max=30V
V_{GS} max=+/-20V
V_{GS} (th)=0.8V/1.5V (min/max)
R_{DS} (ON)=130mΩ (max, V_{GS}=2.5V)
I_D=100mA (TA=25°C)
Ton delay=15ns
Rise time=35ns



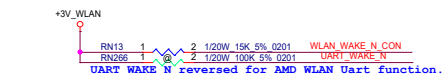
BK requirement, place close to Codec

MOSFET: FDMA8878

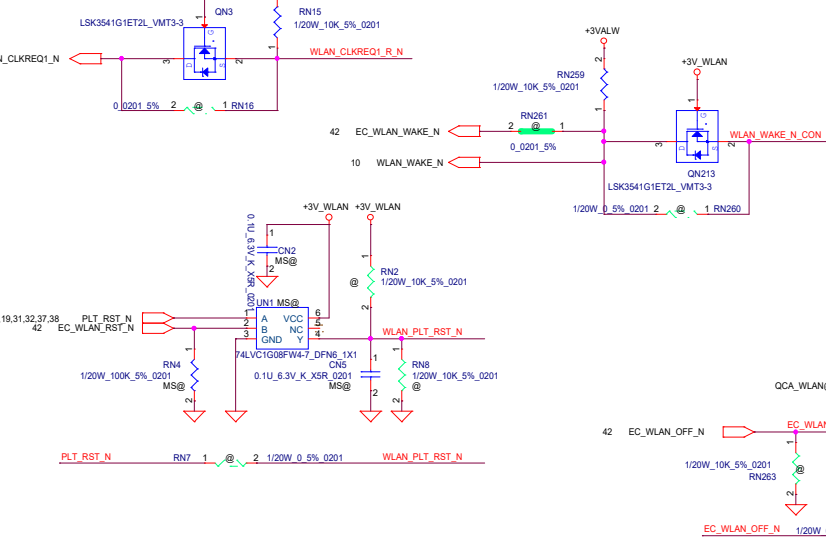
Vds max=30V, Vgs max=+/-20V
Vgs(th)=1.2V/1.8V/3V(min/typ/max)
Vgs=4.5V(With 3Cell B+)
Rds(ON)=16mohm/19mohm(ryp/max, Vgs=4.5V)
Vgs=10V(With 4Cell B+)
Rds(ON)=13mohm/16mohm(ryp/max, Vgs=10V)
Id=9A (TA=25°C)



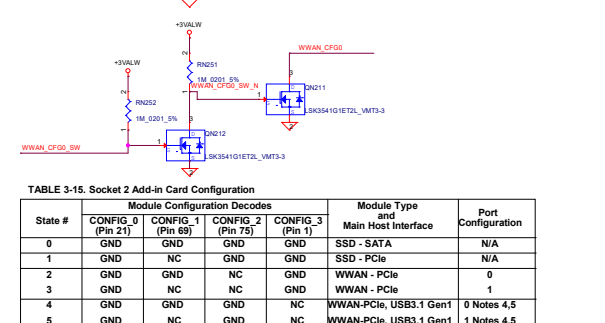
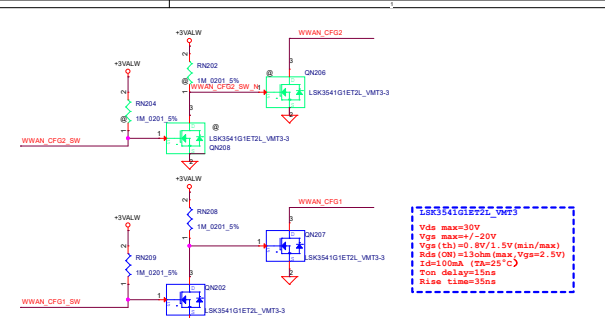
Signal: EC_WLAN_PWRON_N
Voltage Level: 3.3V
L2N7002KWTIG_SOT323-3
Vds max=60V
Vgs max=+/-20V
Vgs(th)=1.2V/2V(min/max)
Rds(ON)=2.7ohm(max, Vgs=5V)
Id=380mA (TA=25°C, t<5s)
Ton delay=3.8ns
Rise time=3.4ns



LSK3541G1ET2L_VMT3
Vds max=30V
Vgs max=+/-20V
Vgs(th)=0.8V/1.5V(min/max)
Rds(ON)=13ohm(max, Vgs=2.5V)
Id=100mA (TA=25°C)
Ton delay=15ns
Rise time=35ns

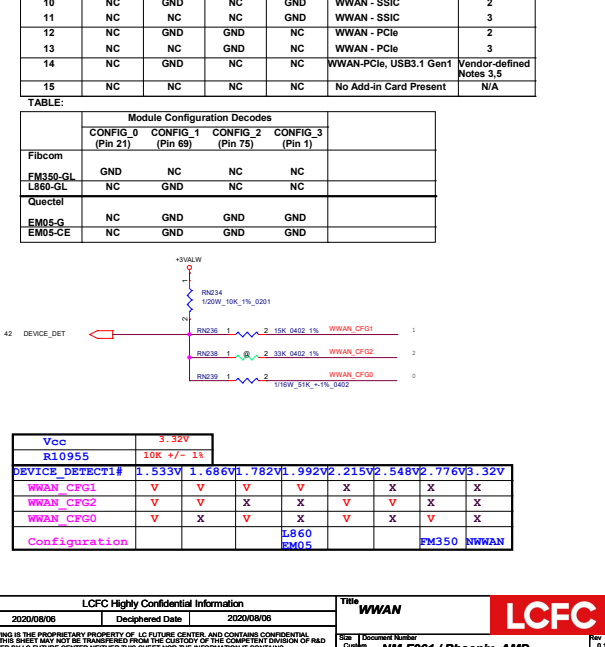


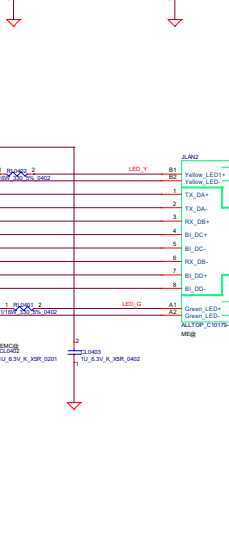
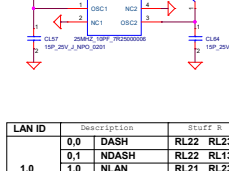
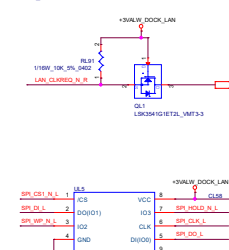
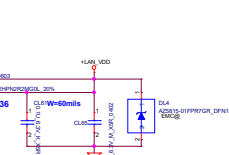
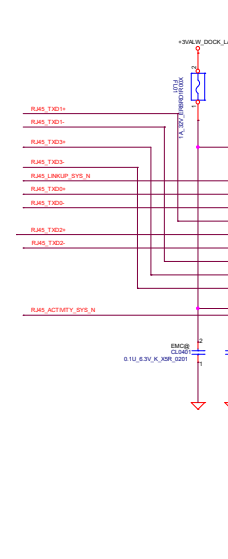
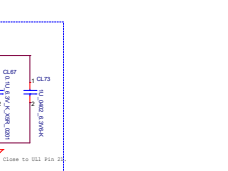
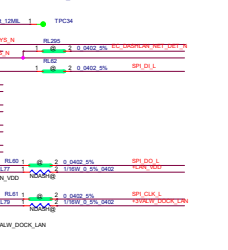
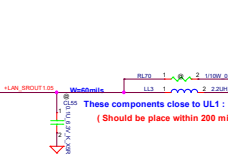
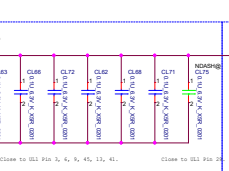
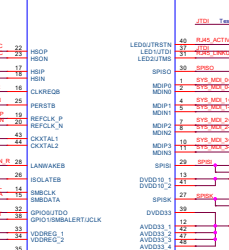
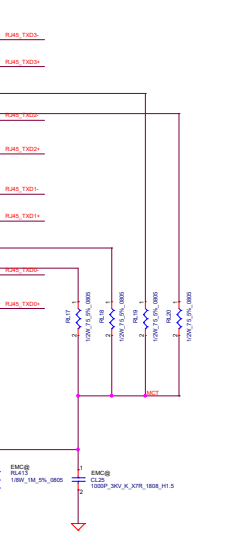
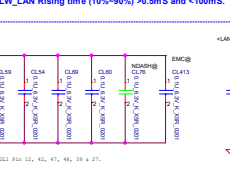
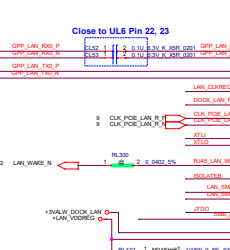
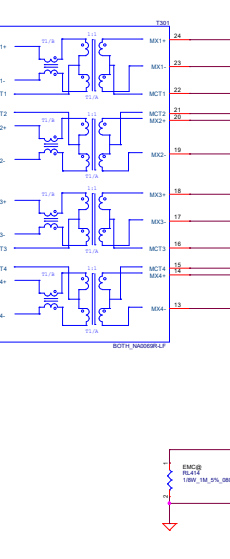
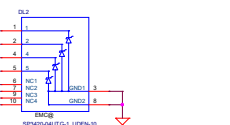
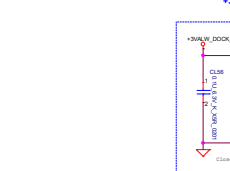
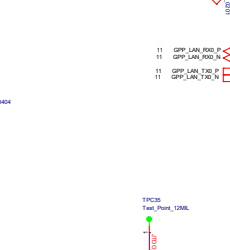
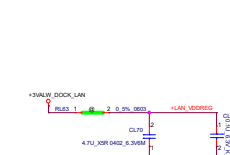
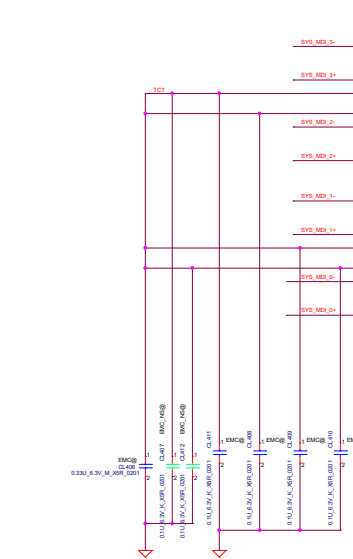
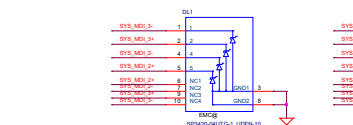
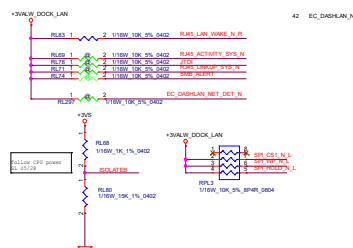
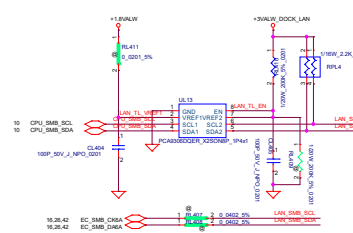
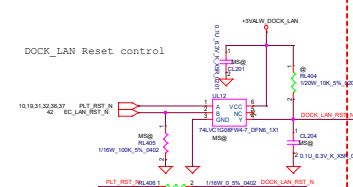
EC_WLAN_OFF with Qualcomm WLAN
GPIO was 1.8V and internal PU,
So EC_WLAN_OFF_N on EC side
should be set with OD without PU



State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	NC	GND	GND	SSD - PCle	N/A
2	GND	GND	NC	GND	WWAN - PCle	0
3	GND	NC	NC	GND	WWAN - PCle	1
4	GND	GND	GND	NC	WWAN-PCle, USB3.1 Gen1	0 Notes 4,5
5	GND	NC	GND	NC	WWAN-PCle, USB3.1 Gen1	1 Notes 4,5
6	GND	GND	NC	NC	WWAN-PCle, USB3.1 Gen1	2 Notes 4,5
7	GND	NC	NC	NC	WWAN-PCle, USB3.1 Gen1	3 Notes 4,5
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	NC	GND	GND	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	NC	NC	GND	WWAN - SSIC	3
12	NC	NC	GND	NC	WWAN - PCle	2
13	NC	NC	GND	NC	WWAN - PCle	3
14	NC	GND	NC	NC	WWAN-PCle, USB3.1 Gen1	Vendor-defined Notes 3,5
15	NC	NC	NC	NC	No Add-in Card Present	N/A

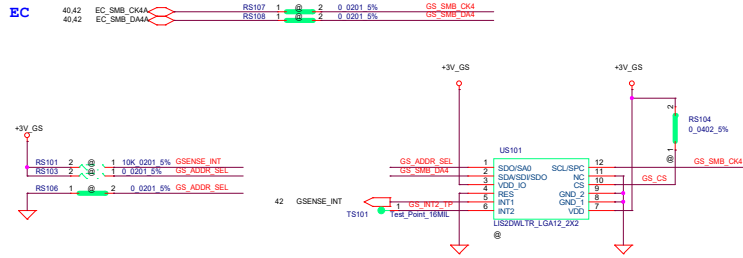
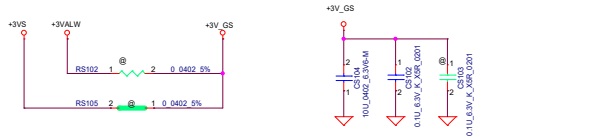
TYPE-B NGFF CARD FOR WWAN





LAN ID	Description	Buffer R
0,0	DASH	RL22 RL23
0,1	NDASH	RL22 RL13
1,0	NLAN	RL21 RL23
1,1	2.5G LAN	RL21 RL13

G sensor#
(On Board)



TABLE

P/N	ADDR_SEL	Address
LIS2DWLTR/ BMA422	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)

TABLE of G-Sensor (U148)	
1	0.000000
2	0.000000
3	0.000000
4	0.000000
5	0.000000
6	0.000000
7	0.000000
8	0.000000
9	0.000000
10	0.000000
11	0.000000
12	0.000000
13	0.000000
14	0.000000
15	0.000000
16	0.000000
17	0.000000
18	0.000000
19	0.000000
20	0.000000
21	0.000000
22	0.000000
23	0.000000
24	0.000000
25	0.000000
26	0.000000
27	0.000000
28	0.000000
29	0.000000
30	0.000000
31	0.000000
32	0.000000
33	0.000000
34	0.000000
35	0.000000
36	0.000000
37	0.000000
38	0.000000
39	0.000000
40	0.000000
41	0.000000
42	0.000000
43	0.000000
44	0.000000
45	0.000000
46	0.000000
47	0.000000
48	0.000000
49	0.000000
50	0.000000
51	0.000000
52	0.000000
53	0.000000
54	0.000000
55	0.000000
56	0.000000
57	0.000000
58	0.000000
59	0.000000
60	0.000000
61	0.000000
62	0.000000
63	0.000000
64	0.000000
65	0.000000
66	0.000000
67	0.000000
68	0.000000
69	0.000000
70	0.000000
71	0.000000
72	0.000000
73	0.000000
74	0.000000
75	0.000000
76	0.000000
77	0.000000
78	0.000000
79	0.000000
80	0.000000
81	0.000000
82	0.000000
83	0.000000
84	0.000000
85	0.000000
86	0.000000
87	0.000000
88	0.000000
89	0.000000
90	0.000000
91	0.000000
92	0.000000
93	0.000000
94	0.000000
95	0.000000
96	0.000000
97	0.000000
98	0.000000
99	0.000000
100	0.000000

Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
BOSCH	BMA422	SA0000C1V00
Miramems	DA6618	SA0000CE000

Table 17. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

Miramems

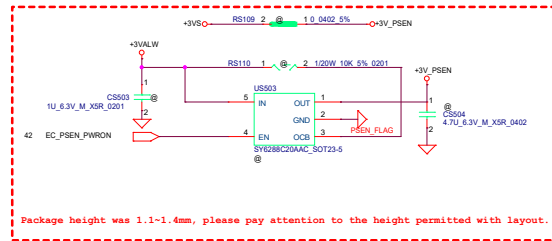
Table 9.I2C Address

SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	W/R
0	1	0	0	1	1	SA0	0/1

Table 10.SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0]–SA0	R/W	SAD+R/W
Read	010011	0	1	01001101(4dh)
Write	010011	0	0	01001100(4ch)
Read	010011	1	1	01001111(4fh)
Write	010011	1	0	01001110(4eh)

P sensor

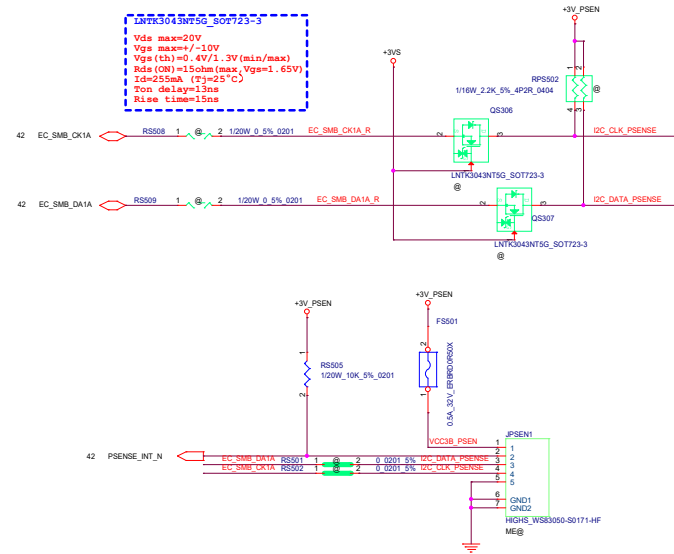


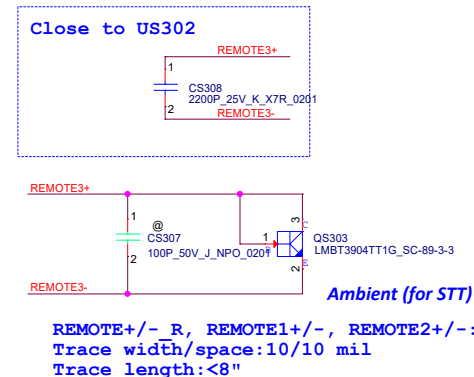
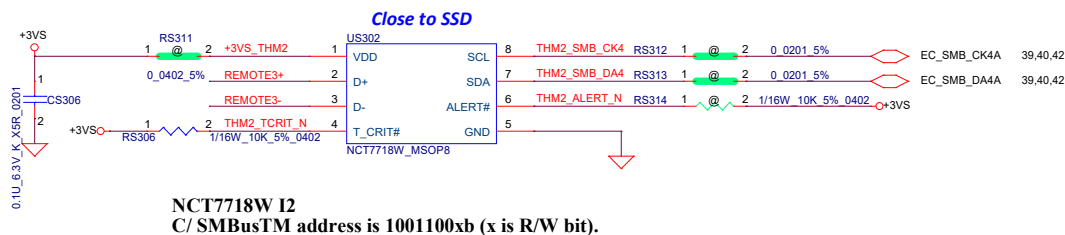
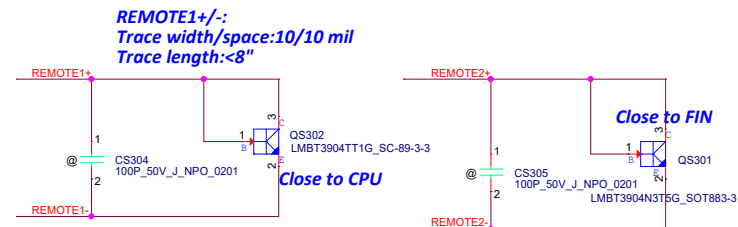
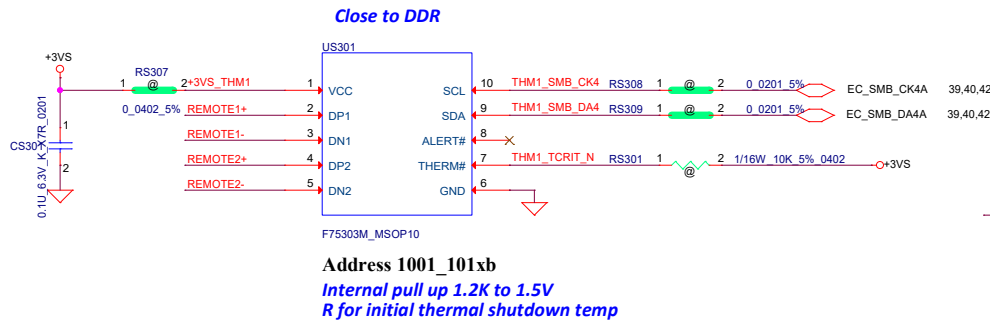
Package height was 1.1~1.4mm, please pay attention to the height permitted with layout.

```

LNTK3043NT5G_SOT723-3
Vds max=20V
Vgs max=+/-10V
Vgs(th)=0.4V/1.3V(min/max)
Rds(ON)=15ohm(max,Vgs=1.65V)
Id=255mA(Tj=25°C)
Ton delay=13ns
Rise time=15ns

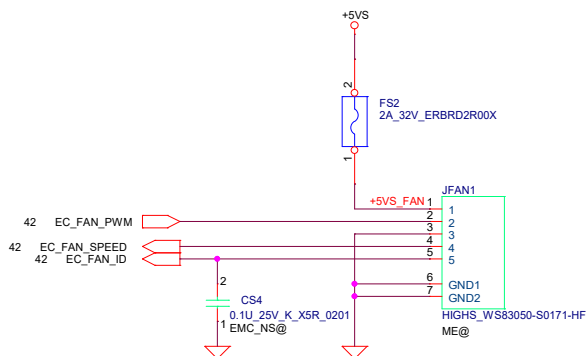
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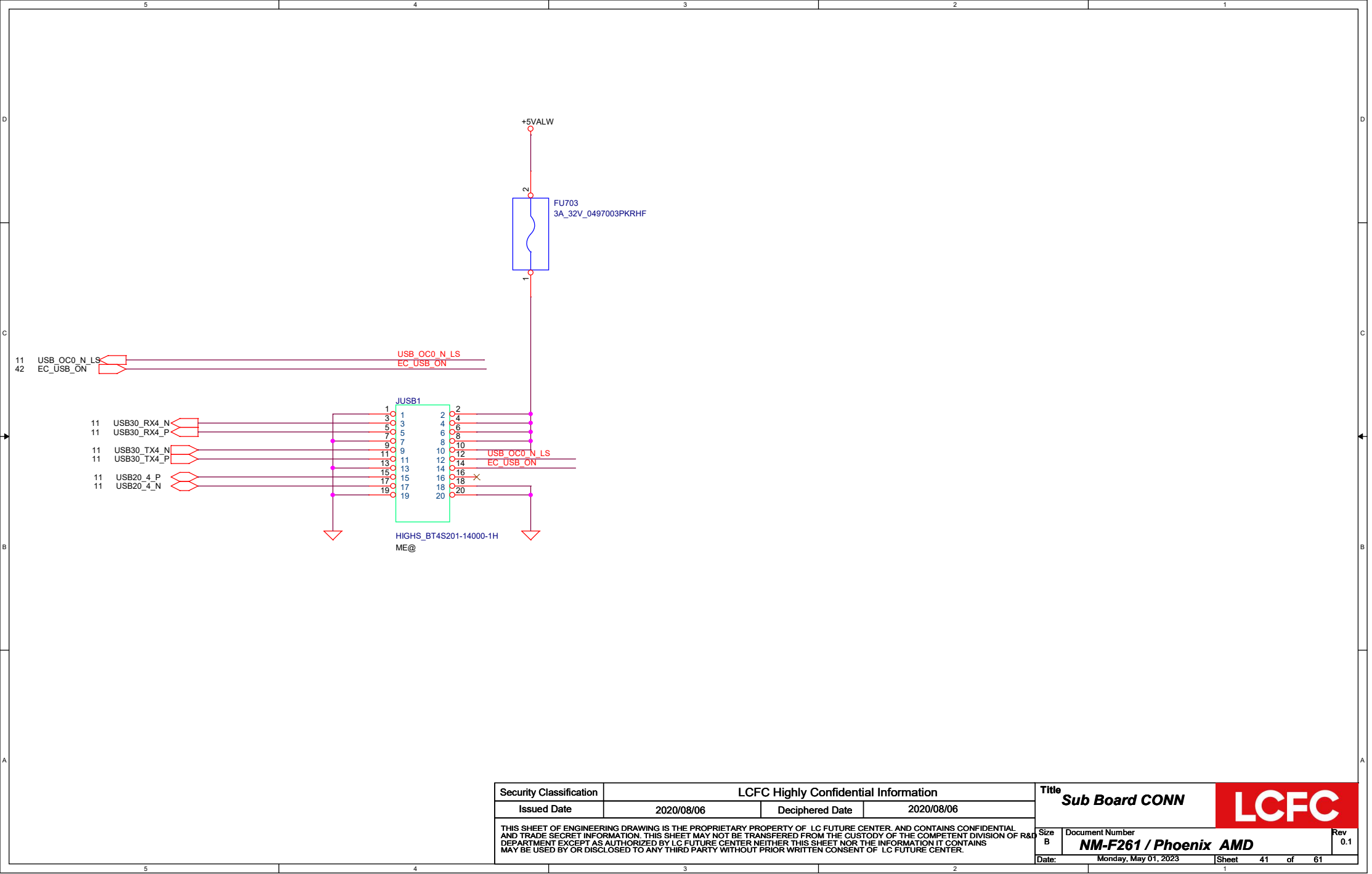
FAN CURRENT
IS 0.5A MAX

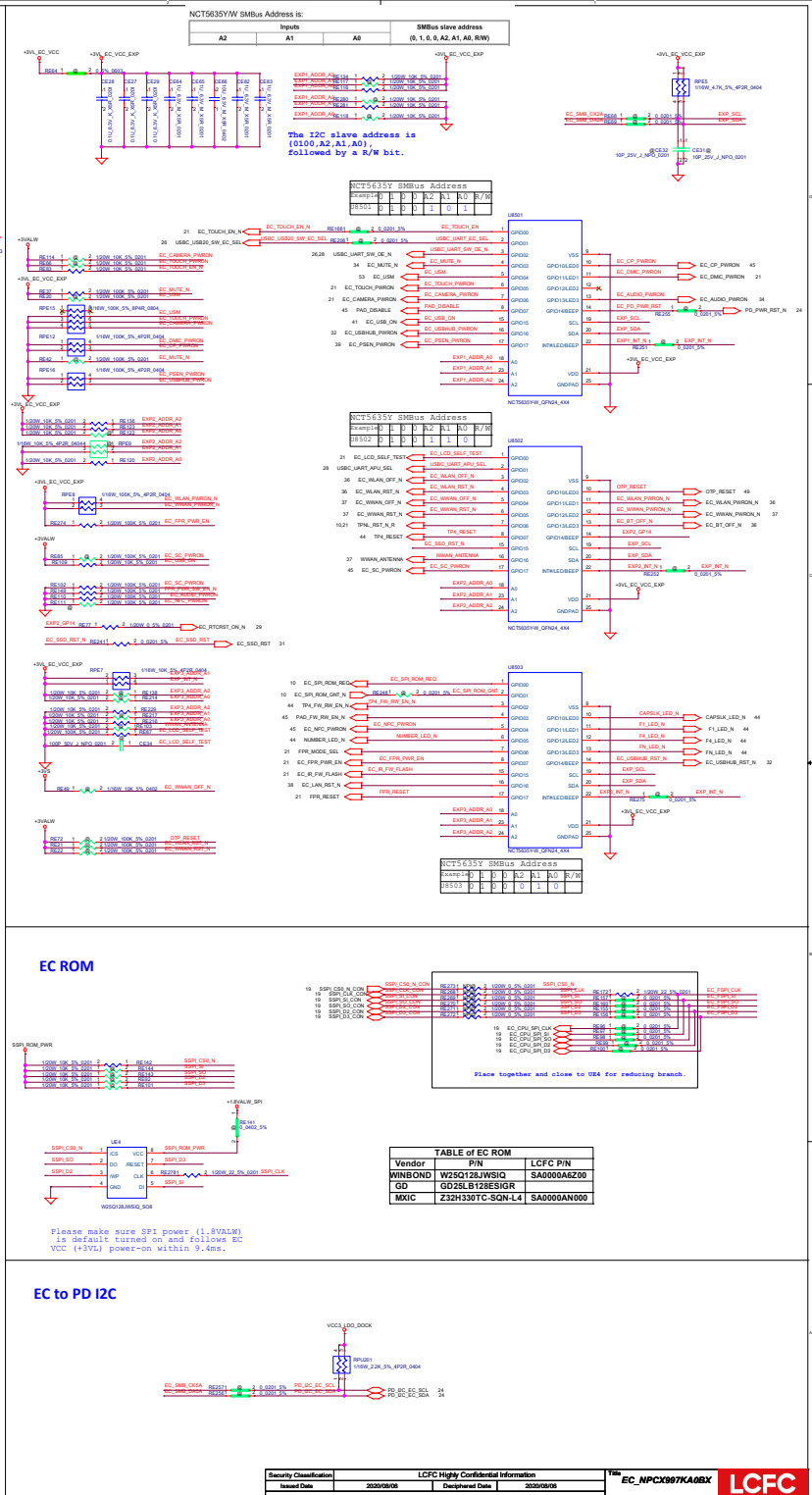
FUSE 2.0A

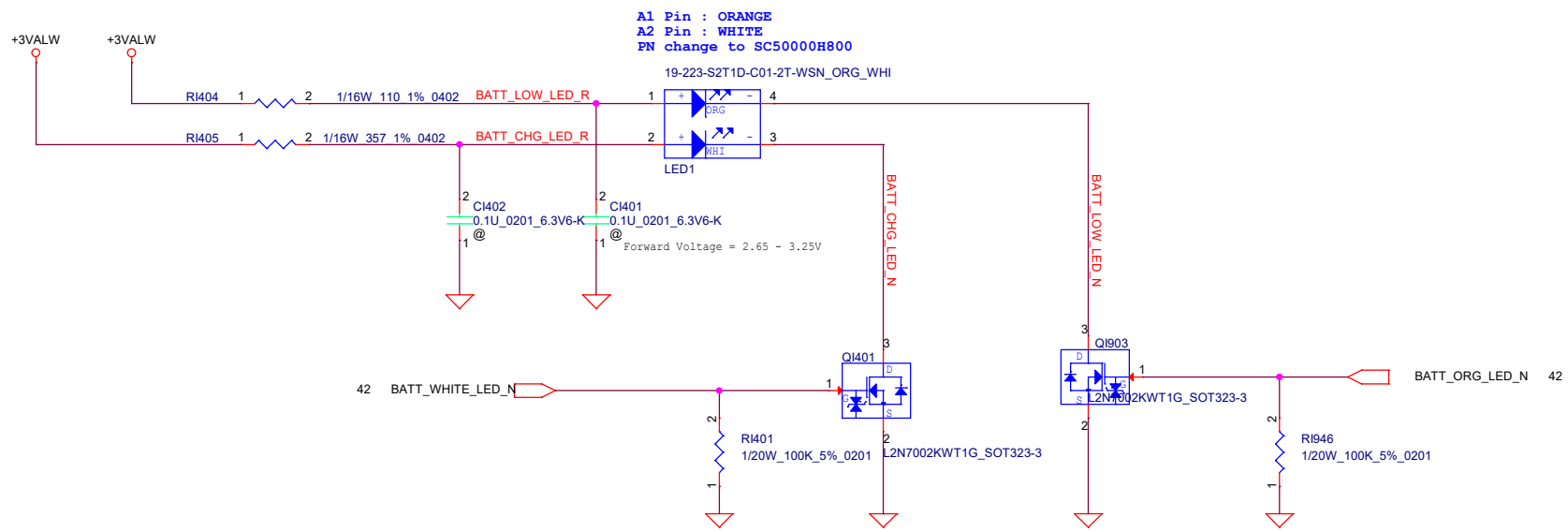


Security Classification		LCFC Highly Confidential Information	
Issued Date	2020/08/06	Deciphered Date	2020/08/06
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Title		LCFC	
Thermal			
Size	Document Number		
Custom	NM-F261 / Phoenix AMD		
Date:	Rev		
Monday, May 01, 2023	0.1		
Sheet 40 of 61			







Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06
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Title		LCFC
BATTERY LED		
Size	Document Number	Rev
B	NM-F261 / Phoenix AMD	0.1
Date:	Monday, May 01, 2023	Sheet 43 of 61

42 CAPSLK_LED_N

42 F1_LED_N

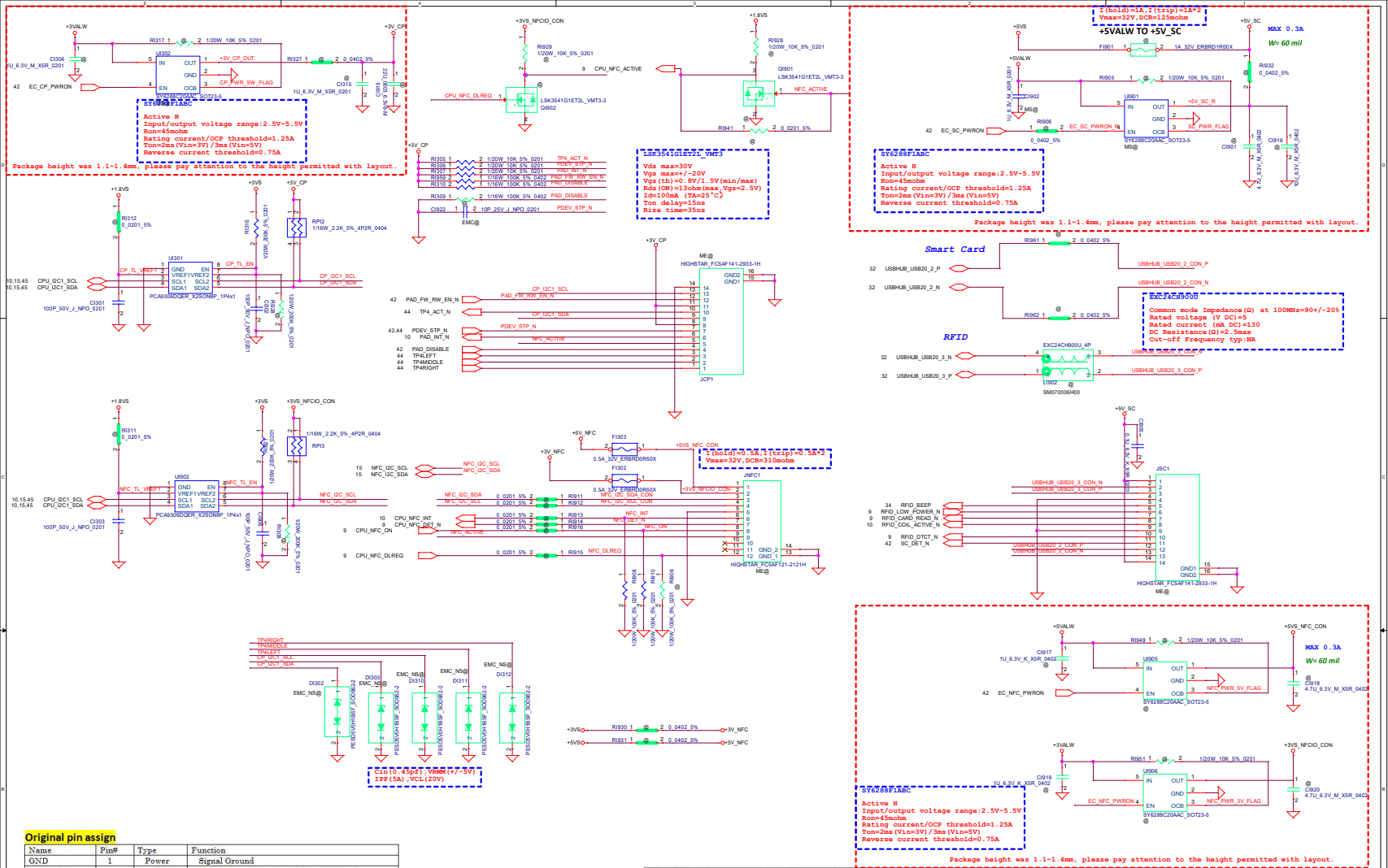
42 F4_LED_N

42 FN_LED_N

42 NUMBER_LED_N

[illegible]

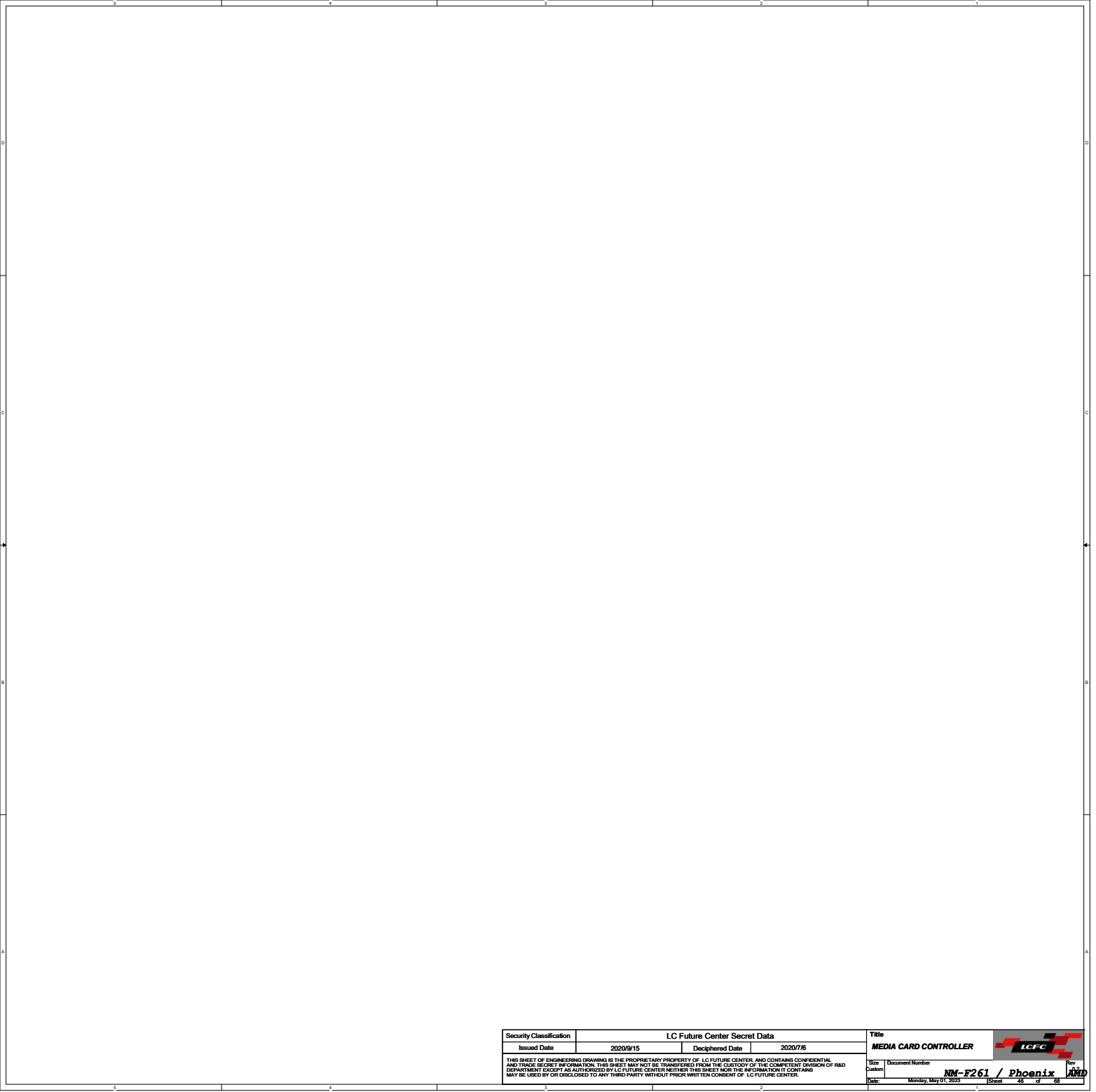
Security Classification		LCFC Highly Confidential Information		Title		KB/KBBL COIN		LCFC	
Issued Date		2020/08/06		Deciphered Date		2020/08/06			
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF: LG LIFUTURE CORP. AND CONTAINS CONFIDENTIAL AND/OR TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LG LIFUTURE CORP. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LG LIFUTURE CORP.</p>						Size		Document Number	
						Date		<p>NM-F261 / Phoenix AMD</p>	
						<p>Monday, May 01 / 2021</p>		<p>Sheet 44 of 61</p>	




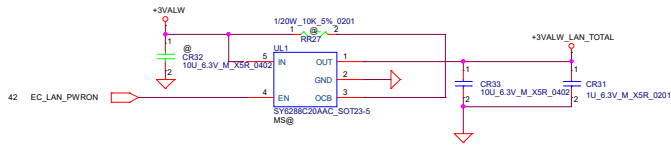
Original pin assign

Name	Pin#	Type	Function
GND	1	Power	Signal Ground
I2C_CLK	2	IN/OUT	I2C Clock to System I2C I/F on CPU/PCB
IPD_GND	3	IN	TrackPoint ground
NC	4		
TP4_ACT	5	IN	TrackPoint Activity status. Please refer to "4.2.8"
I2C_DAT	6	IN/OUT	I2C Data to System I2C I/F on CPU/PCB
Vcc	7	Power	Supply power from system. Power is not supplied when system is in S3, S4, S5 and G5 state. (Refer to electrical requirement)
PDEV_STP	8	IN	This signal is used to disable to report button status and finger status to system when system LCD lid is closed or is in Tent /Stand /Tablet modes (Yoga case). Please refer to "4.2.5 PDEV_STP"
I2C_INT	9	OUT	Interrupt for I2C communication
NFC_Active	10	IN	This signal should use if NFC Antenna is implemented under touch pad PCBA. This signal should be NC or not be used in touch pad PCBA if NFC antenna is not implemented under touch pad PCBA. Please refer to "4.2.6 NFC Active"
PAD_DISABLE	11	IN	This signal is used to disable touch pad. Please refer to "4.2.4 PAD_DISABLE"
TP4LEFT	12	IN	TrackPoint button signal
TP4MIDDLE	13	IN	TrackPoint button signal
TP4RIGHT	14	IN	TrackPoint button signal

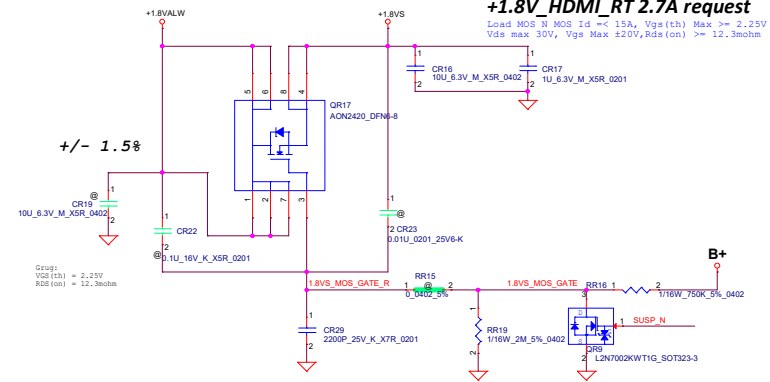
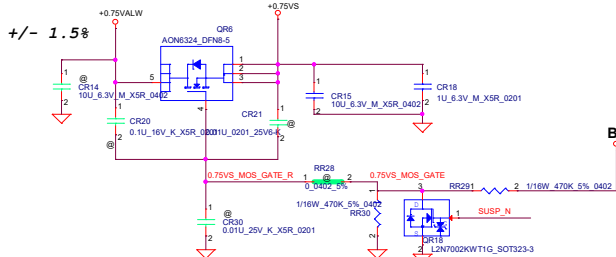
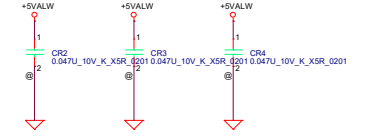
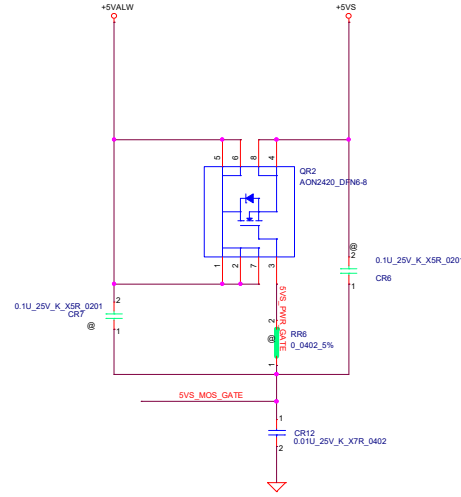
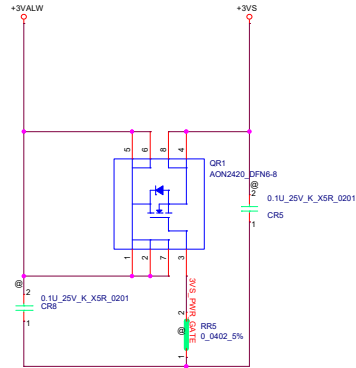
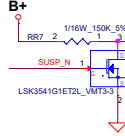
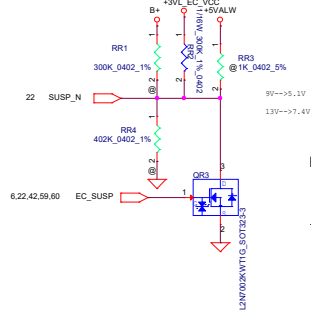
Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V - 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C_SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down (External TX power supply request) (Active high 1.8V level output)
9	TX_PWR_REQ	O	VDD	Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UIICC(1.78V-3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to I/O
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground



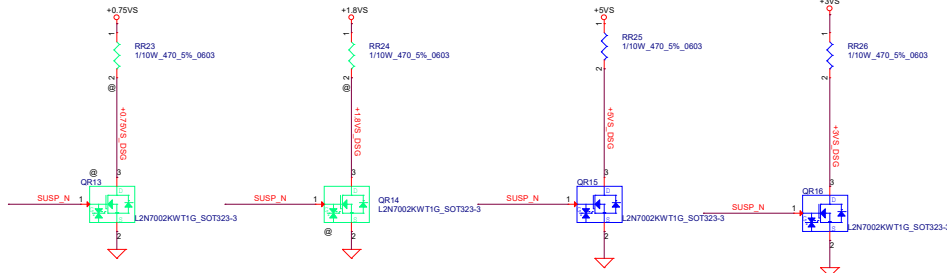
Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		MEDIA CARD CONTROLLER	
2020/9/15		2020/7/6			
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Custom					
Date: Monday, May 01, 2023					Rev
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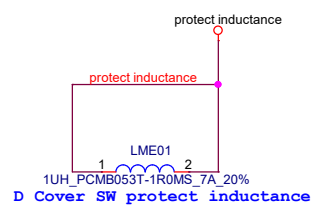
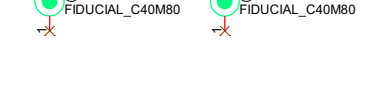
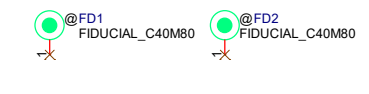
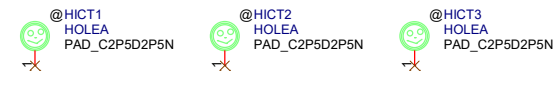
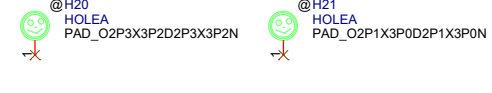
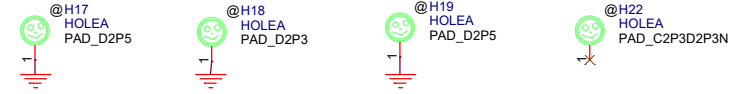
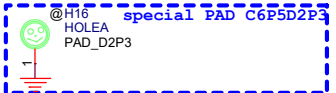
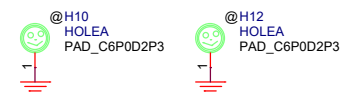
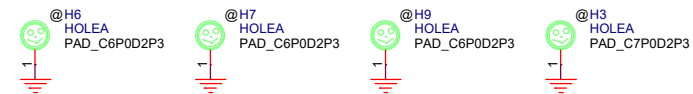


Package height was 1.1-1.4mm, please pay attention to the height permitted with layout.

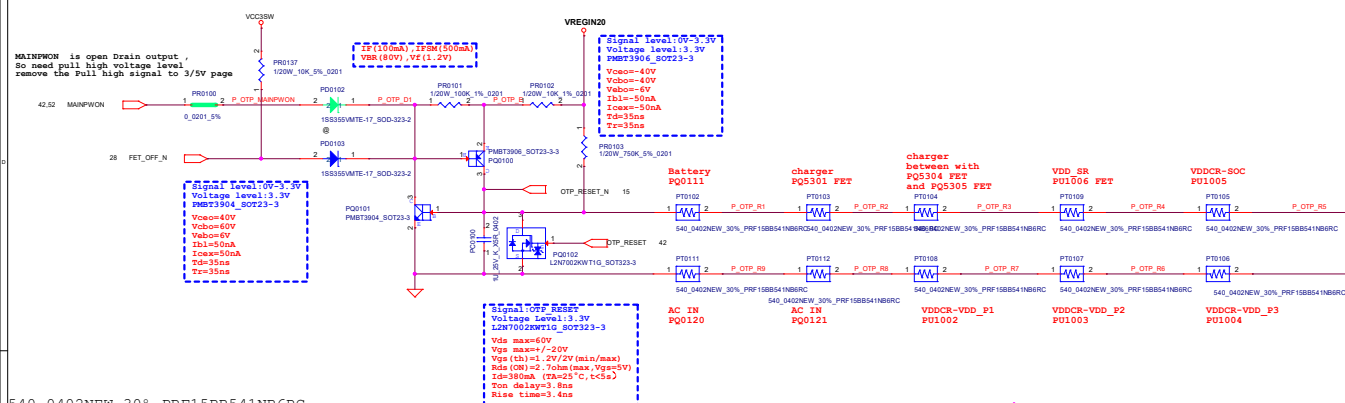


For DisCharge





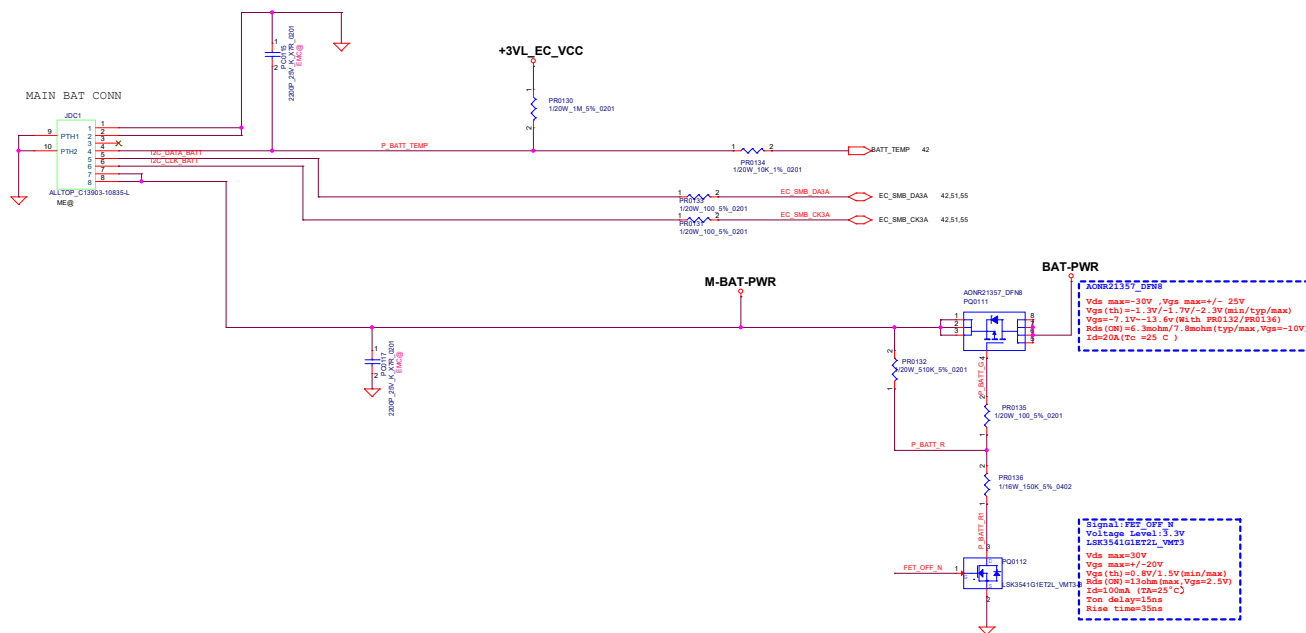
MAINPWON is open Drain output ,
So need pull high voltage level
remove the Pull high signal to 3/5V page



```

540 0402NEW_30%_PRF15BB541NB6RC
25-100Degree
0.54@25 Degree
1.2*0.54*k@85Degree
2*0.54 k@100 Degree
20*0.54 k@120Degree
100*0.54 k@130Degree
350*0.54 k@140Degree
Vbattery min =9V,Vbattery max =12.6V
Vthreshold min=0.65V,Vthreshold min=0.85V,
TotalR ( PTC)*(VBatt-1.25)/(TotalR ( PTC)+750)=0.65V
TotalR ( PTC)=59.8K==110 times 0.54 k
TotalR ( PTC)min=43.72K==80times 0.54 k
Normal run 3Dmark
the max T maybe 85 Degree
the total R PTC= 1.2*0.54*10=12*0.54 k
if only one PTC over 130 degree,
the total PTC is 100*0.54K+11*0.54k,>80*0.54K
and over the min Vthreshold,and active the OTP
if only one PTC over 140 degree,
the total PTC is 350*0.54K>>80*0.54K
,can over the min Vthreshold
and active the OTP
so,the OTP function is ok

```



PRT0110 under CPU botten side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

Security Classification	LCFC Highly Confidential Information		Title	PWR_DGIN/RTC	
Issued Date	2020/08/06	Deciphered Date	2020/08/06	<div style="background-color: red; color: white; padding: 10px; text-align: center; font-size: 2em; font-weight: bold;">LCFC</div>	
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File Name	Document Number	Rev			
Case#	NM-F261 / Phoenix JMS	0.1			
Version			May, 01, 2023	Sheet	46 of 62

Part Reference:
PX5301~PX53**

MLCCs must be placed
symmetrically on Top and Bottom.

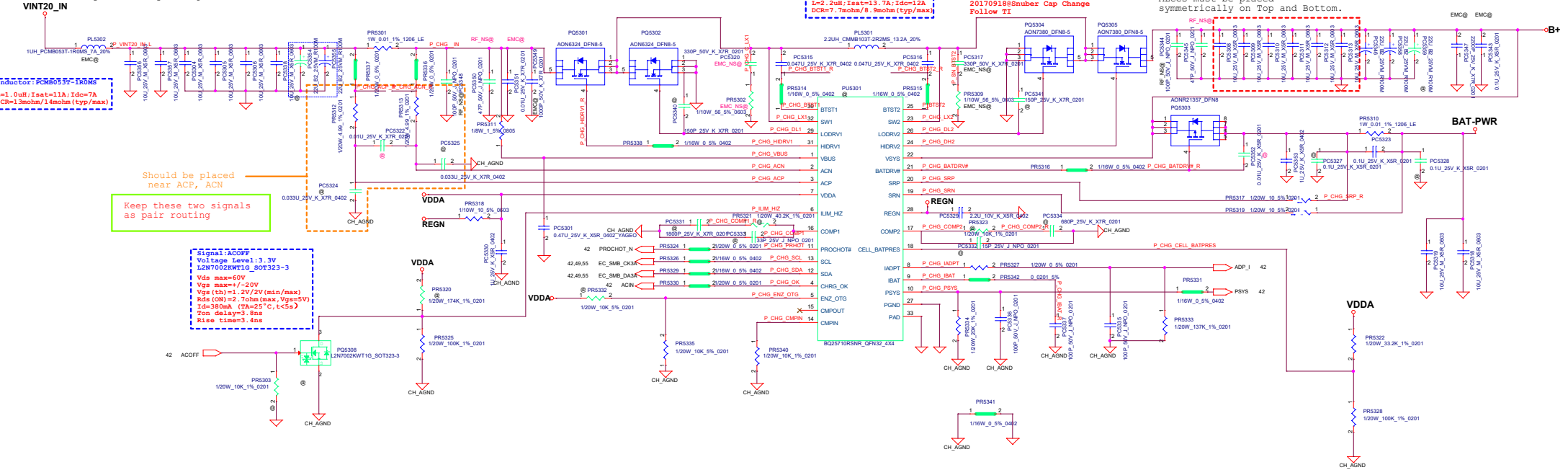
Q1:
Vds max=30V, Vgs max=+- 20V
Vgs(th)=1.2V/1.7V/2.1V(min/typ/max)
Vgs=6V(With BQ25710RSNR)
Rds(ON)=7.3mohm/9.1mohm(typ/max, Vgs=4.5 V)
Id=20A(Tc =25 C)
Q2:
Vds max=30V, Vgs max=+- 12V
Vgs(th)=1.1V/1.5V/1.9V(min/typ/max)
Vgs=6V(With BQ25710RSNR)
Rds(ON)=2.6mohm/3.5mohm(typ/max, Vgs=4.5 V)
Id=12A(Tc =25 C)

Inductor: CDR6053-100MS
L=2.2uH; Isat=13.7A; Idc=12A
DCR=7.7mohm/9.3mohm(typ/max)

AON7380_DFN8-5
Vds max=30V, Vgs max=+- 20V
Vgs(th)=1.4V/1.8V/2.2V(min/typ/max)
Vgs=6V-12V(With RT023782QW-2)
Rds(ON)=8.2mohm/10.5mohm(typ/max, Vgs=4.5 V)
Rds(ON)=5.6mohm/6.8mohm(typ/max, Vgs=10 V)
Id=24A(Tc =25 C)

AONR21357_DFN8
Vds max=30V, Vgs max=+- 25V
Vgs(th)=1.3V/-1.7V/-2.3V(min/typ/max)
Vgs=10V(With BQ25710RSNR)
Rds(ON)=6.3mohm/7.8mohm(typ/max, Vgs=10V)
Id=20A(Tc =25 C)

MLCCs must be placed
symmetrically on Top and Bottom.



IDPM	V(ILIM)	PR5320
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

← LOGIC

CHGT10: Install for BQ25710RSNR
CHGSOUTH8: Install for SC8885SQDER

TABLE of Main/2nd			
C	PU5301	T1 BQ25710RSNR (1st)	Southchip SC8885SQDER (2nd)
ACP	PC5324	0.033u_25V_K_XTR_0402	NO_ASM
ACN	PC5325	0.033u_25V_K_XTR_0402	NO_ASM
COMP1	PR5321	40.2K_1%_0201	1/20W_68K_1%_0201
COMP1	PC5331	1800P_25V_K_XTR_0201	220P_50V_K_XTR_0201
COMP1	PC5333	33P_25V_J_NPO_0201	NO_ASM
COMP2	PR5323	10K_1%_0201	1/20W_27K_1%_0201
COMP2	PC5332	15P_25V_J_NPO_0201	NO_ASM
COMP2	PC5334	680P_25V_K_XTR_0201	330P_50V_K_XTR_0201
ILIM_HZ	PR5320	174K_1%_0201	137K_1%_0201

TABLE of PU5301			
1st	Vendor	P/N	LCFC P/N
2nd	Southchip	BQ25710RSNR	SA00009K300
		SC8885SQDER	SA0000DDA00

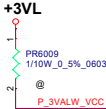
# of CELL	VCELL_PRES	PR5322
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

← LOGIC

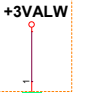
Part Reference:
PX6001-PX60**

TABLE of PU6001			
	Vendor	P/N	LCFC P/N
1st	TI	TPS51393PRJER	SA00009A200
2nd	SILERGY	SYV768BRAC	SA0000CHC00
3rd	Joulwatt	JW5168BQFN	SA0000DFD00

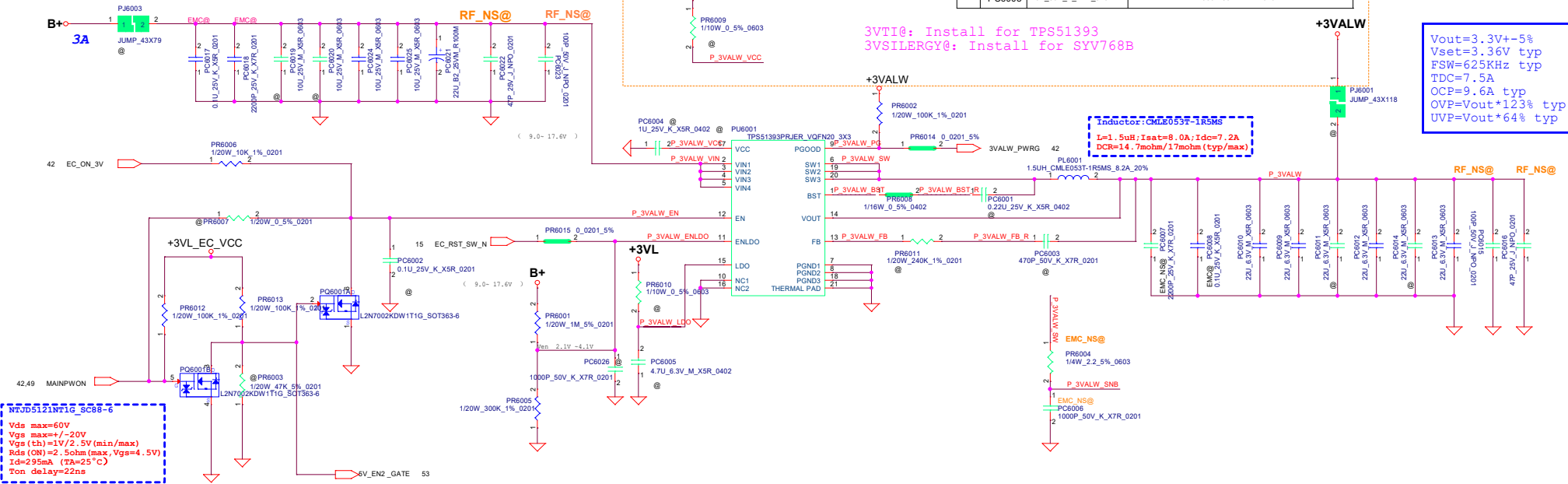
TABLE of Main/2nd/3rd			
IC	PU6001	TI TPS51393PRJER (1st)	Silergy SYV768BRAC (2nd) / Joulwatt JW5168BQFN (3rd)
VCC	PC6004	1U_25V_K_X5R_0402	4.7U_6.3V_M_X5R_0402
VCC	PR6009	NO_ASM	0_5%_0603
LDO	PR6010	0_5%_0603	NO_ASM
LDO	PC6005	4.7U_6.3V_M_X5R_0402	NO_ASM
BST	PC6001	0.22U_25V_K_X5R_0402	0.1U 25V K X7R 0402
FB	PR6011	240K_1%_0201	1K +-1% 0201
FB	PC6003	470P_50V_K_X7R_0201	1000P 50V K X7R 0201



3VTI@: Install for TPS51393
3VSILERGY@: Install for SYV768B



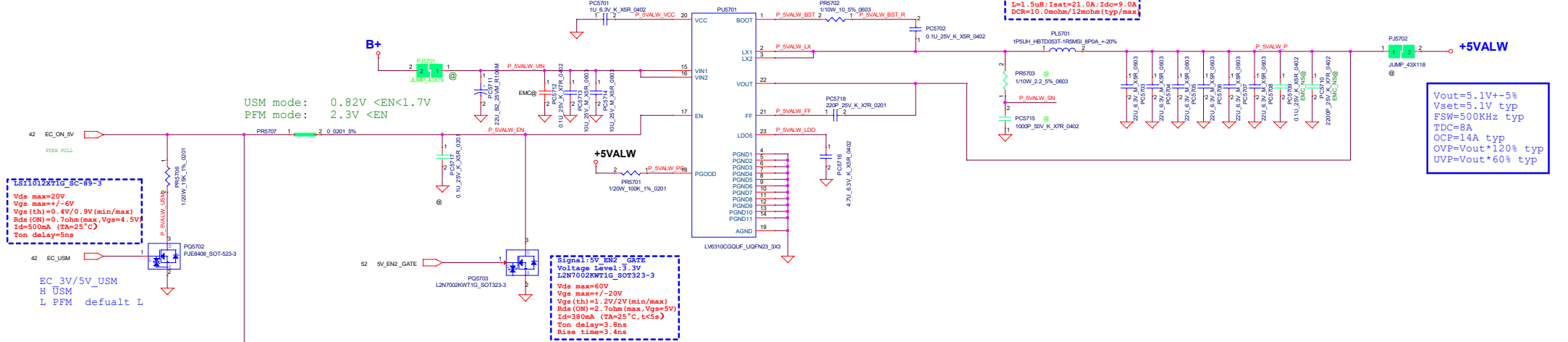
Vout=3.3V+-5%
Vset=3.36V typ
FSW=625KHz typ
TDC=7.5A
OCP=9.6A typ
OVP=Vout*123% typ
UVP=Vout*64% typ



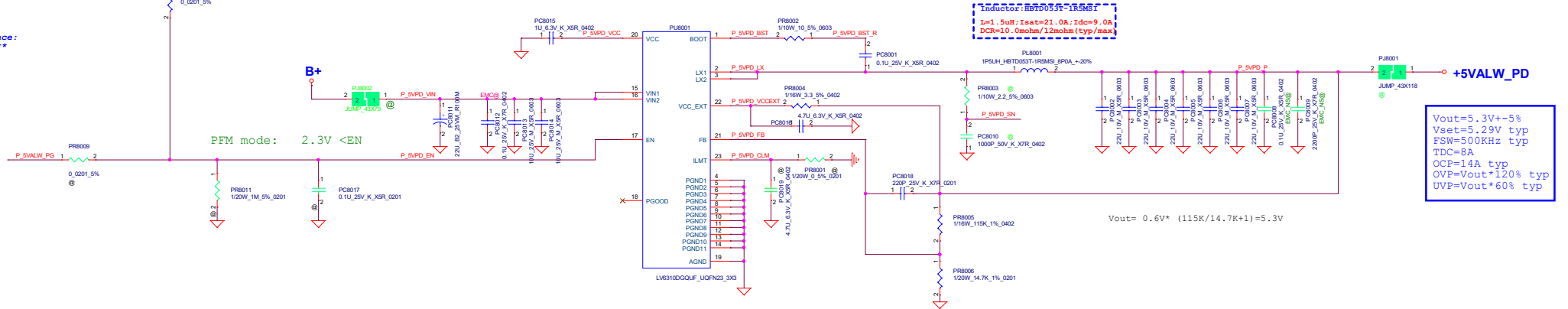
NTUD5121N1IG_SCB8-6
Vds max=60V
Vgs max=+-20V
Vgs (th)=1V/2.5V (min/max)
Rds (ON)=2.5ohm (max, Vgs=4.5V)
Id=295mA (TA=25°C)
Ton delay=22ns

Inductor: CML053T-1R5MS
L=1.5uH; Isat=8.0A; Idc=7.2A
DCR=14.7mohm/17mohm (typ/max)

Part Reference:
PX5701-PX57**



Part Reference:
PX8001-PX80**



BOM Option

IC	PU8001	LVB310GGQF	LVB310CGQF
VCC_EXT	PC8016	4.7U_6.3V_K_XSR_0402	NO_ASM
VCC_EXT	PR8005	1/16W_115K_1%_0402	1/16W_339K_1%_0402
VCC_EXT	PR8006	1/20W_14.7K_1%_0201	1/20W_120K_1%_0201
VCC_EXT	PR8004	1/16W_3.3_5%_0402	1/16W_0_5%_0402
ILMT	PC8019	NO_ASM	4.7U_6.3V_K_XSR_0402

BOM Option

IC	PU8001	JW5138A	JW5138C
VCC_EXT	PC8016	4.7U_6.3V_K_XSR_0402	NO_ASM
VCC_EXT	PR8005	1/16W_115K_1%_0402	NO_ASM
VCC_EXT	PR8006	1/20W_14.7K_1%_0201	1/20W_339K_1%_0201
VCC_EXT	PR8004	1/16W_3.3_5%_0402	1/16W_0_5%_0402
ILMT	PC8019	NO_ASM	4.7U_6.3V_K_XSR_0402

Part Reference:
PX3001~PX30**

Vout=0.9V±5%
TDC=0.6A OCP=3A
Vout=0.5*(I+R1/R2)

Inductor: CMLB0531-R68MS
L=1uH; Isat=3.34A; Idc=2.7A
DCR=29mohm/35mohm (typ/max)

Inductor: CMLB0531-R68MS
L=0.68uH; Isat=10.9A; Idc=10.5A
DCR=7.0mohm/8.5mohm (typ/max)

Vout=1.065V±5%
TDC=7A
OCP=14A
Vref=1.065V
OVP=130% typ
UVP=75% typ
Fsw=700Khz

Vout=1.8V±5%
TDC=0.6A

TABLE : Mode selection for NB705

State	VDD2 (Vref)	VDDQ (Vref)	Res to GND
M1	0.9V	0.3V	0
M2	1.1V	0.6V	90K
M3	1.065V	0.3V	150K
M4	1.065V	0.5V	>230K or Float

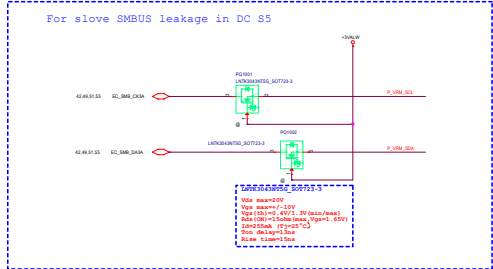
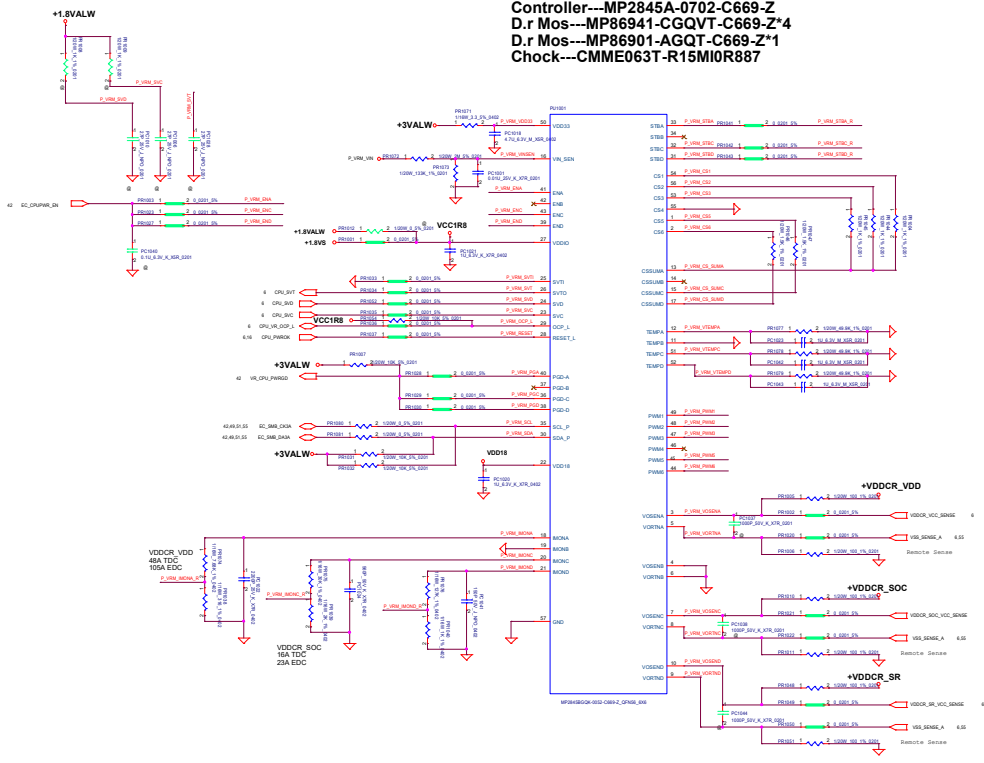
LOGIC

Vout=0.5V±5%
Vset=0.5V typ
Fsw=750KHz typ
TDC=3A
OCP=4A typ
OVP=Vout*125% typ
UVP=Vout*75% typ

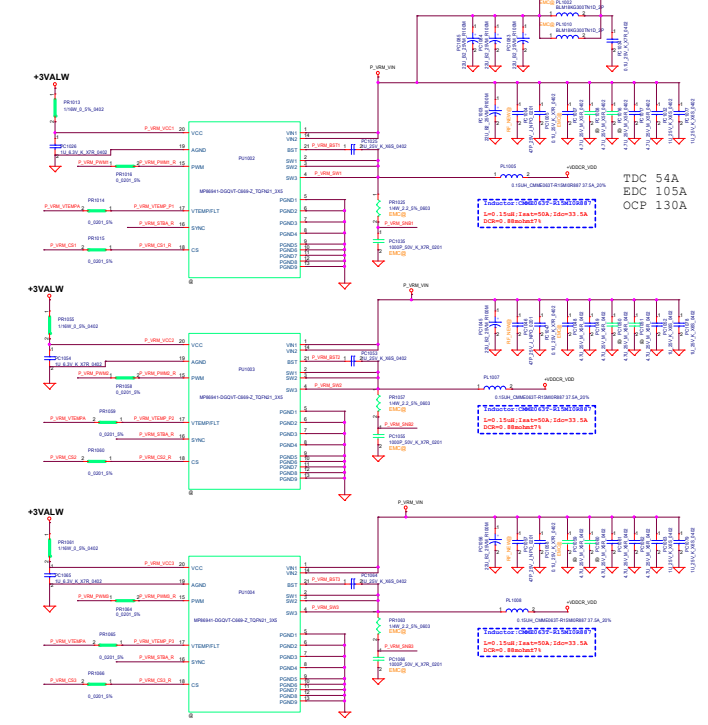
TABLE : Mode selection for NB695A

MODE	LP#	C1	C0	VOUT(V)
150K	1	1	1	0.5

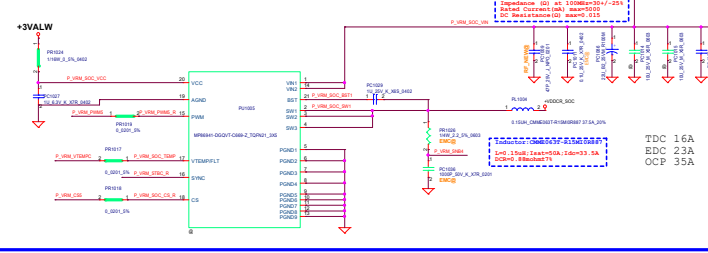
Controller---MP2845A-0702-C669-Z
D.r Mos---MP86941-CGQVT-C669-Z*4
D.r Mos---MP86901-AGQT-C669-Z*1
Chock---CMME063T-R15M10R887



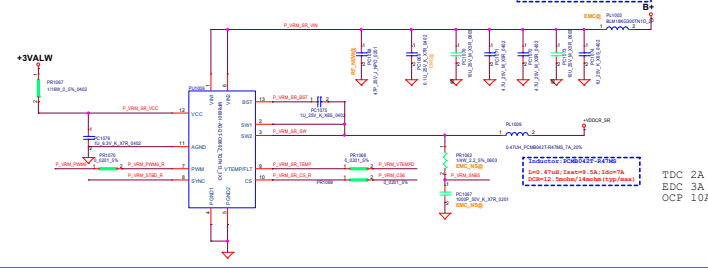
+VDDCR_VDD



+VDDCR_SOC



+VDDCR_SR



Part Reference:
PX1100~PX12**

Place on Bot side

Place on TOP side

Note--Rembrandt
470uF/4.5mohm*7pcs D2+220uF/6mohm D2*4
22uF/0603*12pcs
22uF/0402*40pcs

Rembrandt
470uF/4.5mohm*2pcs D2+220uF/6mohm D2*1
22uF/0603*6pcs
22uF/0402*20 pcs

+VDDCR_VDD

+VDDCR_SOC

Place on VR side

All BU(on bot side beside CPU)

All BU(on bot side beside CPU)

+VDDCR_VDD

+VDDCR_SOC

All BU(on top side under CPU)

All BU(on top side under CPU)

Place on VR side

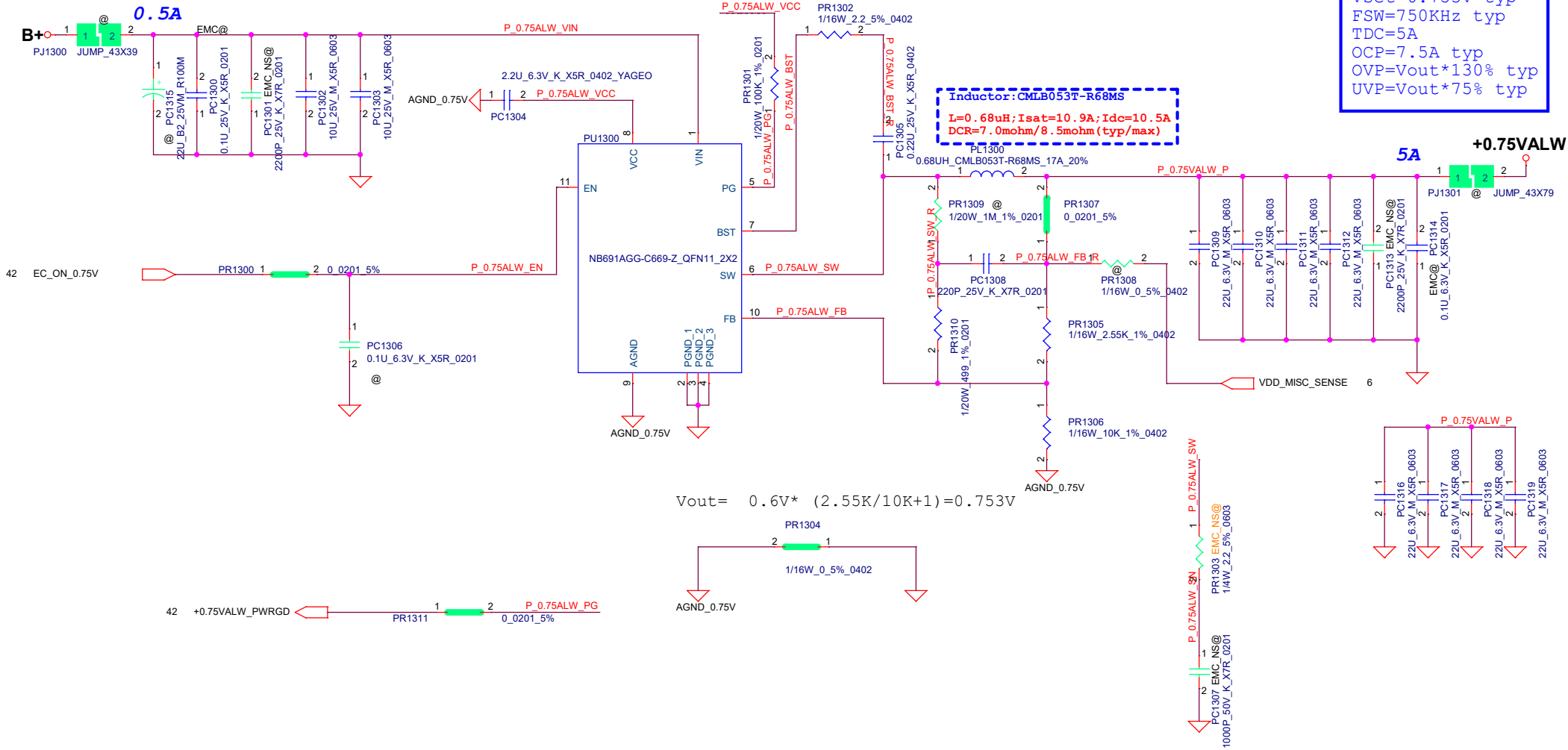
Place on VR side

+VDDCR_SR

Rembrandt
22uF/0603*8pcs
10uF/0402*2pcs

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Date		Monday, May 01, 2023		Sheet		56		of 62	

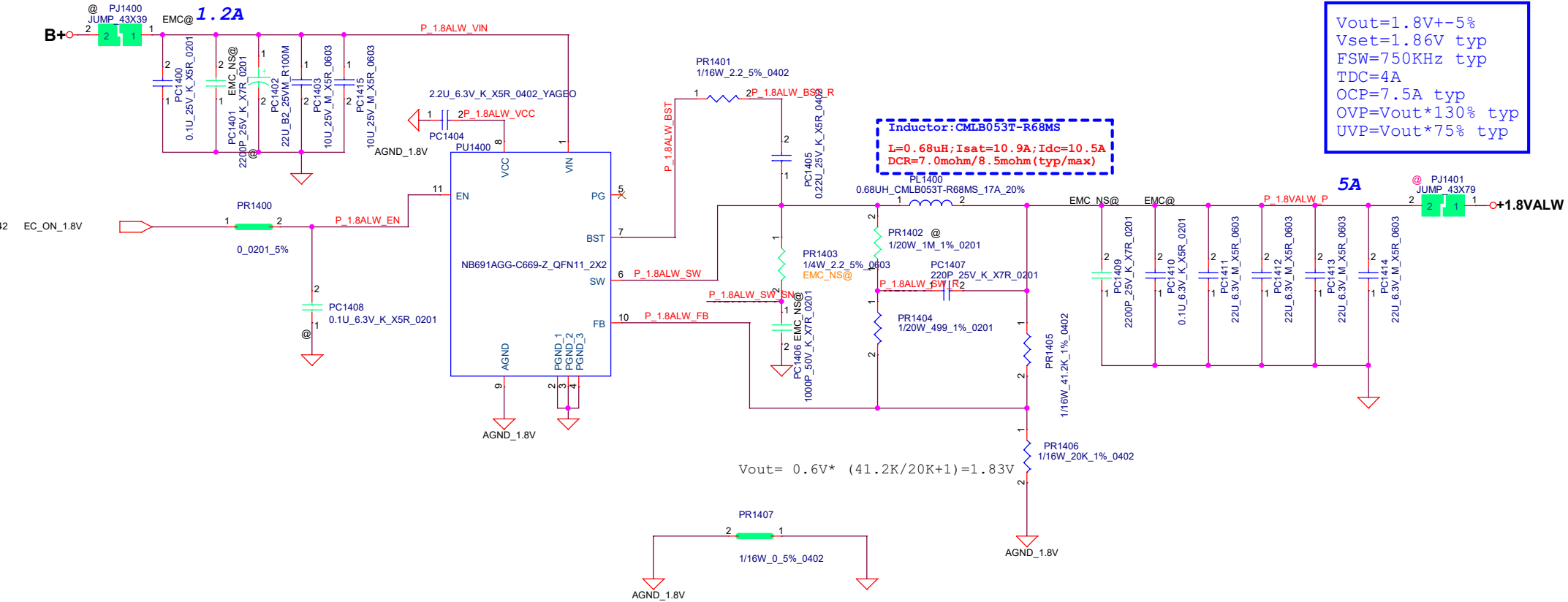
Part Reference:
PX1300~PX1399



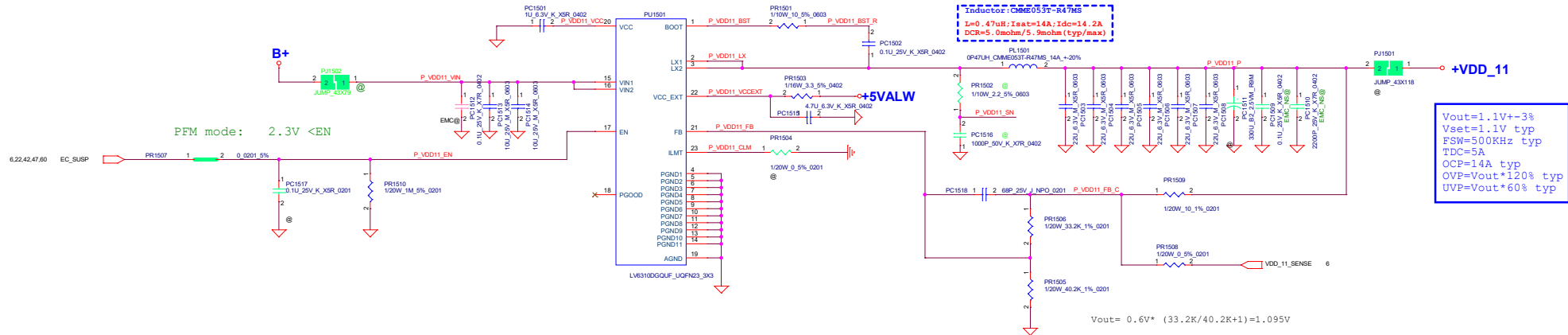
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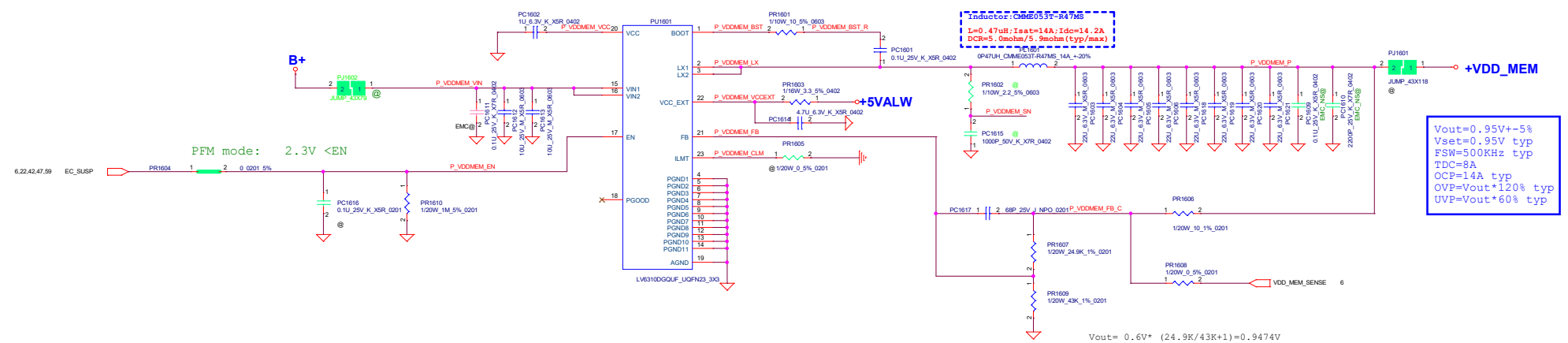
Part Reference:
PX1400~PX1499



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Part Reference:
PX1600~PX1699



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